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Planar Fully-Depleted-Silicon-On-Insulator technologies: Toward the 28 nm node and beyond

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ABSTRACT

This paper presents a comprehensive overview of the research done in the last decade on planar Fully-Depleted-Silicon-On-Insulator (FDSOI) technologies in the frame of the joint development program between IBM, ST Microelectronics and CEA-LETI. In particular, we review the technological developments ranging from substrate engineering to process modules that enable functionality and improve FDSOI performance over several generations. Various multi Vt integration schemes to maximize the benefits of the thin BOX FDSOI platform are discussed. Manufacturability as well as scalability concerns are highlighted and addressed. In addition, this work provides understanding of the performance/power trade-offs for FDSOI circuits and device variability. Finally, clear directions for future application-specific products are given, demonstrating that FDSOI is an attractive CMOS option for next generation high performance and low-power applications.

1. Introduction

The semiconductor industry has scaled down feature sizes relentlessly for more than 50 years doubling the density every 18 months, with significant advantages in speed, power consumption and cost. In spite of major efforts to continue the scaling trend, conventional device architecture reached its limit when variability and short-channel effects became impossible to control. Increased channel doping to control short channel effects led to increased junction leakage and higher random doping fluctuations. In short, it became impossible to turn off conventional bulk MOSFETs at small gate lengths [1,2]. New device architectures with ultra-thin body channels were introduced to improve electrostatics. Specifically, FinFETs and planar FDSOI enabled scaling to continue beyond the 28 nm node. These device architectures overcome the barriers of conventional devices since they do not rely on channel doping to control short channel effects. Electrostatics in these devices is controlled by the thin silicon film channel thickness. In fact the DIBL and subthreshold slope improve for a given gate-length as a function of thinner silicon channel thickness.

Planar FDSOI is fabricated using a thin Si film (less than 10 nm) on a buried oxide insulator (BOX). In the last decades, FDSOI has been demonstrated to offer additional features and benefits compared to other options including: (i) total dielectric isolation to lower junction leakage and capacitance and latch-up immunity; (ii) undoped channel to reduce threshold voltage variation and enable higher mobility; (iii) ultra-thin BOX (~25 nm) to improve electrostatics, and enable back-biasing for Vt tuning and power-performance trade-off optimization; (iv) multiple work-function metal gates and ground-plane doping for multi Vt devices; (v) simple co-integration of bulk and FDOI devices allowing for legacy bulk IP preservation; (vi) simple planar layout similar to conventional bulk technology, allowing for re-use of most of the previous generation bulk CMOS FEOL modules and simple migrating of digital libraries and designs to FDSOI [3]. ARM-based cores operating up to a record frequency of 3 GHz [4,5] have been demonstrated at the system level using 28 nm node ground rules [6]. FDSOI technologies have begun to reach mainstream manufacturing. The market place presence of FDSOI is further expanding with foundry, partners, ecosystem and IP providers.

In this paper, we review the main research steps enabling FDSOI going from concept to demonstration of SoC in chronological order. We mainly focus on activities made in the frame of the joint development program between IBM, ST Microelectronics and CEA-LETI,

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showing that significant achievements have been made possible thanks to intensive R&D contributions in the last decades from both academia and industries. Not only we will introduce main technological solutions allowing for 28 nm Ultra-Thin-Body and -Box (UTBB) FDSOI technologies in production, but we will also discuss the extendibility of FDSOI by reviewing the main innovations for the next generations of FDSOI.

2. FDSOI technology evolution

In order to fulfill the requirements for low-power and high-performance applications, FDSOI device architecture processes and materials have been optimized for each technology node. It should also be mentioned that since FDSOI electrostatics is driven by namely by the ratio of gate length to channel thickness, as the gate-length decreases the channel thickness should also decrease [7,8]. Thinning the BOX also leads to improved electrostatics because the thinner BOX allows the back gate to be more effective in terminating electric fields originating in the source during the off state of the transistor. Fig. 1 describes one potential FDSOI technology roadmap showing key performance boosters for 28 nm, 14 nm and 10 nm nodes respectively [9]. Note that another version of the FDSOI roadmap was recently presented [10]. Although the timing of the introduction of some of the elements may differ, both roadmaps have the same key features including performance boosters and function enhancing modules. In this paper we describe many of the innovations as well as the research that was used to shape and define these roadmaps.

2.1. Toward a 28 nm FDSOI technology

Double gate and fully depleted devices have historical roots going all the way back to at least the mid 1980's. One of the first reports of a double gate device structure was by Sekigawa in 1984 [11]. In 1988 Fukuma presented work that included the concept of thin BOX, intrinsic channel with ground plane doping underneath [12]. Although the FDSOI concept was not completely ignored, little research was done for quite some time in this area mainly due to the fact that conventional devices were meeting scaling and performance requirements for technology applications. However, it is interesting to note that some applications have very demanding requirements for ultra-low power operation which can be achieved using FDSOI. In fact in 1998 Oki announced an ultra-low power technology based on FDSOI. Oki's FDSOI was used for several generations in the well-known solar powered watch. As scaling became more challenging and gate dielectric scaling slowed there was an increased effort to move fully depleted devices forward [13–16].

More recent research on FDOSI devices focused to replace conventional bulk MOSFET showed several promising results. Several important works including Lolivier et al. [17] who showed ultra-thin SOI nMOSFETs with silicon thinned down to 8 nm, gate length as short as 10 nm, totally salicided source/drain (engineered with pocket implantation). The use of an undoped channel allowed to get rid of dopant and thickness fluctuations. This was one of the results that provided evidence that FDSOI was potentially scalable to very aggressive technology nodes. Other key results include the thin BOX device design work by Numata and Takagi in 2004 [18], one of the first demonstrations of FDSOI using a thin BOX substrate by Tsuchiya et al. in 2004 [19]. Gate stack for fully depleted devices is a key aspect of the FDSOI device design. In fact, since FDSOI has no channel doping, including halo implants, band edge metal gate electrode do not produce appropriate V_t's in FDSOI devices. Another important FDSOI gate stack study was that of Doris et al. in 2005 [20]. This work demonstrated a high performance FDSOI CMOS technology featuring metal gate electrodes and high-k gate dielectrics. The FDSOI channels were thinned down to 14 nm by oxidizing and wet etching bonded SOI wafers. Devices were isolated by a shallow trench scheme. The BOX thickness was 145 nm. Several different gate materials and processes were evaluated. Interfacial layers were formed either by chemical oxidation or thermal nitridation. The high-k dielectric for all stacks was 25 Å of MOCVD HfO_2. The gate electrode materials were PVD and ALD metal or metal nitrides. The gate stack was topped with a-Si. A plasma etch process capable of stopping on the high-k layer was used to pattern the gate stack. To maintain the fully depleted channel, halo and well doping were completely eliminated. Source–drain extensions were formed with low energy arsenic (nFET) and boron (pFET) implants. A cross sectional image of a typical FDSOI metal gate high-k transistor is shown in Fig. 2. Work-function tuning was accomplished by materials and process modification to achieve appropriate threshold voltages for FDSOI CMOS. The gate stacks exhibited an extremely thin effective inversion thickness (T_{inv}) down to 14 Å with a gate leakage current of 0.2 A/cm^2. This represented a six order of magnitude leakage reduction compared to poly/SiO_2. By optimizing the gate stack, the highest unstrained electron mobility was realized (207 cm^2/V s at E_{eff} = 1 MV/cm) at T_{inv} = 14 Å (see Fig. 2). Drive currents of 1050 μA/μm and 770 μA/μm at I_{off} of 90 nA/μm and 28 nA/μm were achieved for nMOS and pMOS respectively. FDSOI metal gate high-k ring oscillators and SRAM cells with 50 nm gate length achieving a static noise margin (SNM) of 328 mV at Vdd = 1.2 V were demonstrated (see Fig. 2). The significance of this work was that for the first time a gate stack with suitable properties for FDSOI was shown. Specifically, high k metal gate with low gate leakage, thin T_{inv}, high mobility and appropriate threshold voltage was presented. This breakthrough in gate stack technology forms the basis of FDSOI gate technology for 28 nm node.

A major barrier for FDSOI to become mainstream CMOS was the fact that FDSOI device characteristics strongly depends on the SOI thickness and it was difficult to obtain SOI substrates with uniform SOI thickness to meet the device variability requirement. Progress on wafer uniformity were being pursued by several groups. As early as 2000, Ito et al. presented results using ELTRAN technology showing the feasibility of a 50 nm BOX [21]. These substrates were used for many of the initial demonstrations that required thin silicon and thin BOX. Wafer substrate processing significantly improved and FDSOI thickness uniformity with less than 1 nm across wafer SOI thickness variation were already demonstrated in 2009 [22]. The key substrate parameters including BOX thickness uniformity, silicon thickness uniformity and surface roughness continued to improve and are now readily available from several wafer suppliers meeting remarkably demanding specifications in volume production [60,61].

It is well known that one of the major benefits for FDSOI is greatly improved Vt variation from reduced random doping fluctuation. Since the FDSOI channel is undoped there are no dopants to cause RDF. Thus it was widely anticipated that FDSOI would enable significant improvement in Vt variation. Several research groups, including Asenov and others [63], performed simulations to predict the benefit in Vt variation for undoped channel FDSOI. Ohtou et al. published particularly insightful simulation results for thin BOX FDSOI variability in 2007 [23]. Several researchers presented experimental results demonstrating the Vt variation benefit around the same time as these simulation results were published. In 2008, the improved Vt variation in undoped FDSOI channels (due to reduce random dopant fluctuation effects) was shown [24–26]. One of the several examples of outstanding matching performance is shown (A_{Vt} = 0.95 mV μm) in Fig. 3 [25].

One of the first works demonstrating SOI/hybrid bulk was by Chen et al. in 2005 who presented an SOI/hybrid bulk integration

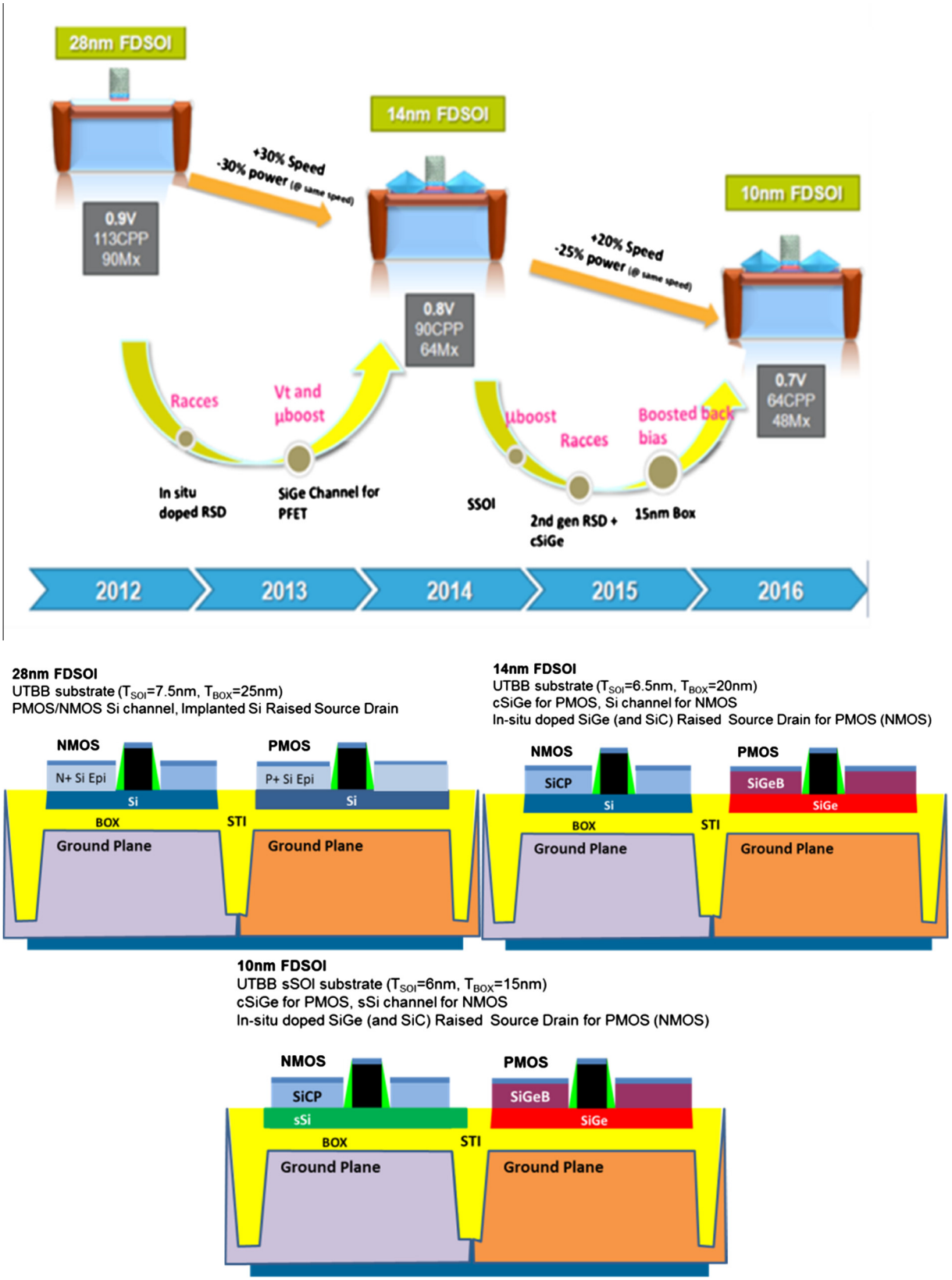


Fig. 1. FDSOI scaling and performance boosters roadmap [8,9] and schematic pictures of the 28 nm, 14 nm and 10 nm FDSOI CMOS technology nodes.

scheme [27]. This initial demonstration and others paved the way and provided inspiration for future work. In 2009, Fenouillet et al. [28] showed multiple Vt operation with ultra-thin BOX (see Fig. 4). The FDSOI devices were processed on 300 mm UNIBOND™ SOI wafers with BOX thicknesses ranging from 145 nm down to 10 nm. The final Si film thickness was around 8 nm with nominal gate-length of 32 nm. The use of a thin silicon film coupled with a thin BOX and ground plane (GP) allowed short channel effect

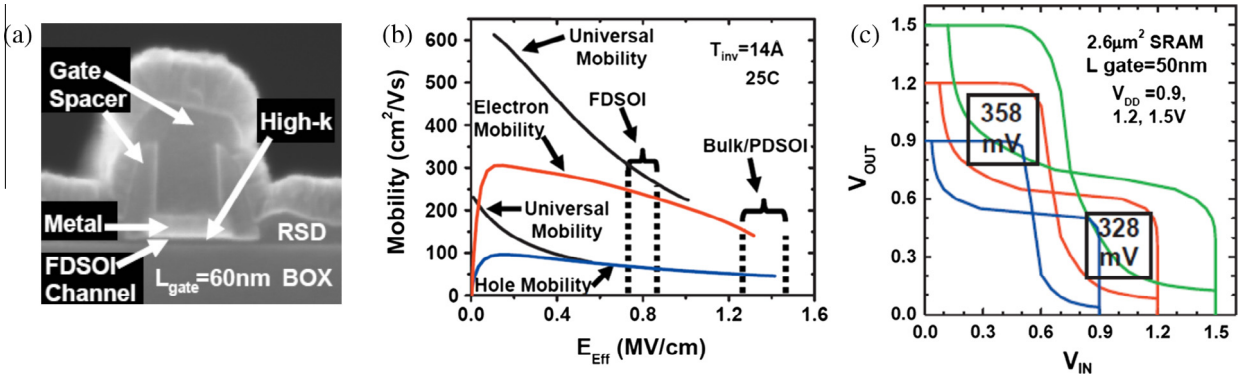


Fig. 2. (a) Cross section of a typical FDSOI transistor prior to silicide. After [20]. (b) Electron and hole mobility vs. Eff (T_{inv} = 14 A). Dashed lines represent the Eff operating ranges. After [20]. (c) SRAM cell showing SNM of 328 mV at *V*dd = 1.2 V. After [20].

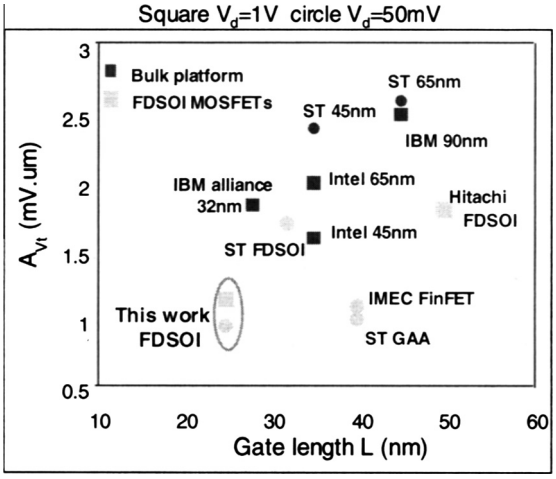


Fig. 3. Summary of A_{Vt} literature results, after [25]. A_{Vt} is defined as $\sigma_{Vt} = A_{Vt}/(W \cdot L)^{0.5}$.

improvement by reducing the lateral electrostatic coupling between the source and the drain. A multi-Vt strategy to enable high and low Vth applications based on the use of UTBOX and appropriate Ground Plane, with a single gate electrode for PMOS and NMOS was presented. By using high Vt devices, for the first time a 2 Mb SRAM with 0.374 μm² cell size @*V*dd 1.4 V was demonstrated. In the same work, the feasibility of a hybrid FDSOI/bulk co-integration on ultra-thin BOX (25 nm) was shown. The report showed FDSOI devices in the top silicon region integrated with I/O's and ESD devices fabricated in the handle wafer under the BOX. A TEM showing FDSOI and Bulk co-integrated devices is shown in Fig. 4.

UTBB devices with a 25 nm-thick oxide BOX, channel thickness T_{Si} ~8 nm, L_g = 25 nm and spacer = 16 nm (consistent with 22 nm node requirements) were demonstrated (Fig. 5) by Liu et al. in 2010 [29]. The process flow featured: STI formation, ground plane implantation and annealing, gate-first high-k metal gate, offset space formation, RSD Epi and implanted S/D. The NFET received a compressive liner to enhance electron mobility. Excellent SCE control and *I*on (N/P) of 470/480 μA/μm were achieved at *V*dd = 0.9 V, with a corresponding off-state current (I_{off}) (N/P) = 2/1.5 nA/μm. The PFET performance was among the best reported for UTBB. A Vt shift of 80 mV was observed when Vbb was varied from 0 V to 0.9 V on both N/P-type GPs, with excellent Vt rolloff down to L_g = 21 nm. This demonstrated the importance and promise of the UTBB structure for multi-Vt and power management applications. Without GP, a low A_{Vt} of 1.27 mV μm was measured (Fig. 5) due to the absence of random dopant fluctuation (RDF) in the channel region. The A_{Vt} with GP was 1.32 mV, suggesting that RDF resulting from GP implantation had little impact on A_{Vt}.

The extremely thin film used in planar FDSOI devices (below 6 nm for 20 nm gate length) poses challenges for advanced processing in particular, junction formation by implantation. Implanted ions have a high probability to create irreversible lattice damage in the thin silicon which in turn dramatically degrades the performance. N-MOSFETs are especially affected as n-type dopants are known to induce more implantation defects. In [30,31], the limits of extension formation by ion implantation into an extremely thin SOI were explored and solutions to alleviate these issues were presented. Three ion implantation based schemes were explored for FDSOI N-MOSFET devices targeted for the 20 nm node (see Fig. 6(a)). It was shown that amorphization of the thin SOI is a key issue for the implant pre RSD scheme (named Extension first – XF) [32]. Both the use of a liner or implant after RSD growth allows alleviating this issue. On the other hand, extension first

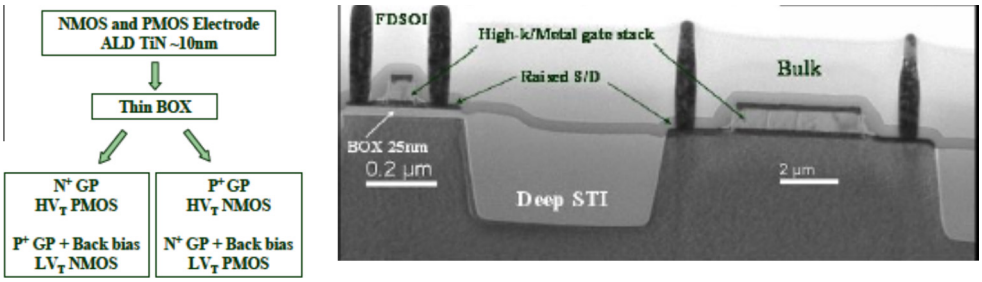


Fig. 4. Left: Threshold voltage strategy for high and low Vt requirements. Right: TEM cross-section of the hybrid FDSOI/bulk co-integration in an SRAM cut periphery. The BOX thickness is 25 nm. After [28].

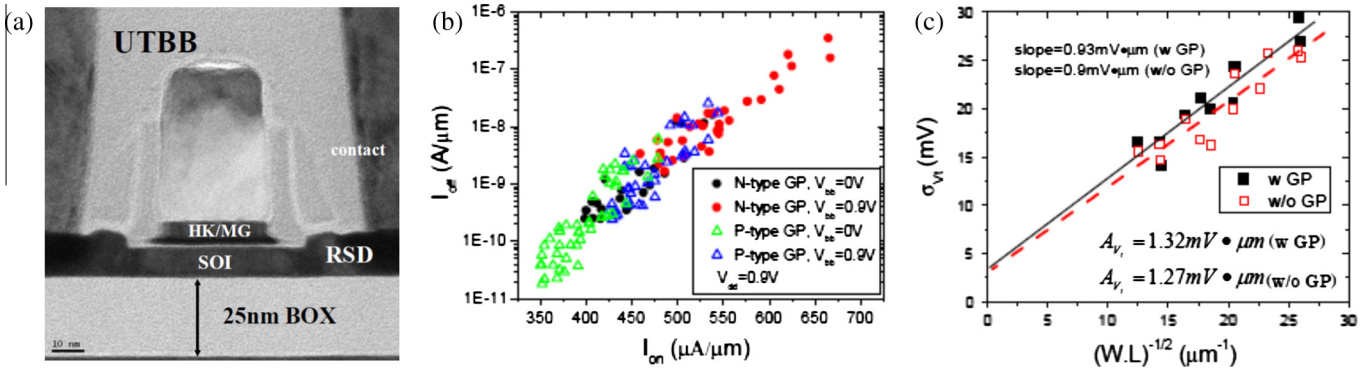


Fig. 5. (a) TEM cross-sections of UTBB featuring 25 nm L_G [29]. (b) UTBB NFET I_{on}–I_{off} showing clear Vt modulation by GP polarity and Vbb [29]. (c) Measured A_{Vt} with/without GP showing a small impact from GP RDF [29].

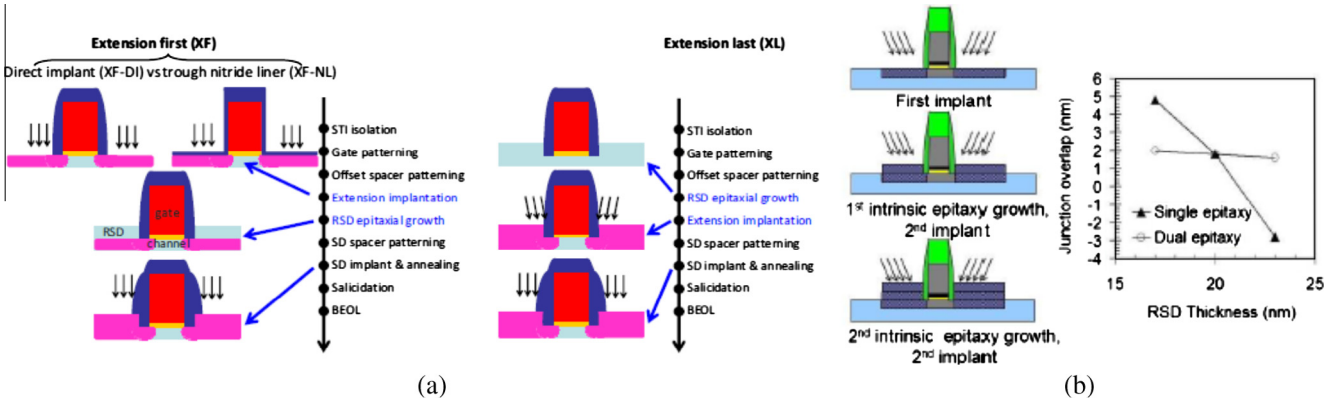


Fig. 6. (a) Process flow of the three I^2 schemes. In XF scheme (left), the dopants are implanted in the thin Si film either directly (XF-DI) or through a nitride liner (XF-NL) and then the RSD is grown. In XL, the dopants are implanted after RSD epitaxy. In terms of device design, the three schemes are expected to lead to different dopants and defects profiles. After [31]. (b) Mitigation of variability with the use of a two-step epitaxy scheme. After [30].

scheme did not retain any evidence of the implant defects created close to the junction after full processing. It was also demonstrated that at the wafer scale the extensions last scheme exhibited high sensitivity to RSD height in terms of gate overlap. Variability was thus the key issue for the implant after RSD scheme which can be alleviated by good process controls and by the use of a two-step epitaxy scheme (see Fig. 6(b)).

One key SoC component for any device architecture is a multi-Vt scheme. In order to make complex circuits for any applications a variety of threshold voltage devices are needed. A multi-Vt strategy featuring a thin BOX substrate with backplane doping (BP) and back biasing (Vb), was realized in 45 nm FDSOI technology (see Fig. 7) [64]. This method can be implemented using a single metal gate which results in process simplification and cost savings. It is also very attractive due to the fact that the forward (FBB)/reverse (RBB) back biasing techniques previously used in conventional bulk technologies can be re-used. Fig. 7 shows the different NMOS/PMOS Vt configurations implemented. For NMOS, the HVT and LVT options were based on a p-type BP set to 0 V and n-type BP set to Vdd, respectively. In this early approach, the SVT option did not include BP and the back bias (Vb) is set to 0 V. For the PMOS device, complementary BP doping type and biasing were applied. All of these devices can be simply co-integrated in a circuit thanks to their configuration which avoids forward biasing PN junctions in the substrate. Fig. 7 also shows the large Vt range obtained by back biasing in NMOS and PMOS LVT family. The effectiveness of back biasing in order to achieve Ion improvement by 45% for LVT options at an I_{off} of 23 nA/μm (and a leakage reduction by 2 decades for the HVT one, not shown) was assessed. In addition, fully functional 0.299 μm^2 SRAM bitcells with 290 mV SNM at 1.1 V and Vb = 0 V operation were obtained. Ring oscillators and 0.299 μm^2 SRAM bitcells were also demonstrated.

The effectiveness of the conventional bulk reverse and forward back biasing approaches to manage the circuit static power and the dynamic performance was presented. The significance of this work was that it presented a systematic study of one of the key differentiating and enabling pieces of the FDSOI or UTBB platform, namely the back gate module.

As previously stated, an extremely useful feature of UTBB is back biasing. Back biasing enables threshold voltage tuning and higher drive currents by forward biasing the channel-drain junction. Liu et al. [33] reported a detailed study of back bias (Vbb) impact on UTBB devices with a gate length of 25 nm and BOX thicknesses of 25 nm and 10 nm, respectively, and a channel thickness of ~6 nm. In the integration flow, the gate and spacer RIE were optimized to minimize the loss of the SOI and to facilitate epitaxial silicon growth. After the second spacer formation, a multi-step implantation was used to reduce the link-up resistance between extension and S/D. Vt modulation by Vbb across a wide temperature range, from −40 °C to 125 °C was reported. The device electrostatics and reliability, under various Vbb were investigated. This work concluded that the short channel effect is well maintained across the bias points. NFET GIDL and HCI both improved when negative bias was applied. The Vbb effect on ring oscillators' (ROs) performance, based on 100 nm contacted gate pitch (CPP), and on a 0.08 μm^2 6-T SRAM, based on 80 nm CPP, were also demonstrated for the first time. Clear RO performance/leakage tradeoff and SRAM static noise margin (SNM) modulation by Vbb

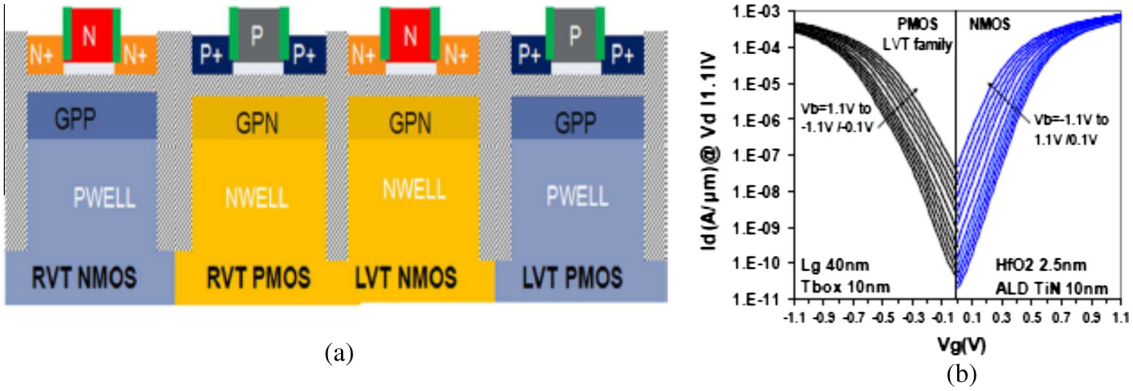


Fig. 7. (a) FDSOI Multi-Vt device strategy [64]. (b) NMOS and PMOS LVT family Id(V_g) curves for variable V_b and L_g 40 nm [64].

were observed. SNM of 206 mV was achieved at Vdd = 0.9 V (Fig. 8). This was one of the first comprehensive reports showing experimental results for the influence of back biasing on aggressively scaled transistors and circuits in an aggressive CPP. Indeed, 28 nm FDSOI technology design choices were made based on all these early works.

Using the middle of line and back end process from the ISDA Common Platform conventional bulk 28 nm node technology offering, the 28 nm FDSOI technology platform for high-speed low-voltage digital applications was established [6]. FDSOI devices were fabricated on substrates with silicon top layer of 12 nm on top of a 25 nm Buried-Oxide. The final channel thickness was 7 nm. The process flow features included STI for device isolation, well implant, back-plane implant for Vt adjustment, NOSOI for SOI/Bulk hybridation, high-k/metal gate first process, offset spacer, epitaxy of raised S/D, LDD implant, spacers, SD implant, RTP spike and DSA annealing, NiSi salicidation, PMD and contacts. The 7 nm undoped thin channel FDSOI along with outstanding junction control enabled excellent electrostatics to support transistors with physical gate-lengths scaled down to 24 nm. Leveraging FDSOI back-side gate capability, a Ground-Plane (GP) implantation was developed to tune the Vt. In order to accurately adjust the threshold voltage for the entire devices suite the Logic and SRAM had different GP doping. The HK/MG process was optimized and used as an additional parameter to control Vt of thin and thick gate oxide devices simultaneously for both N and PFETs. Low VT (LVT) and

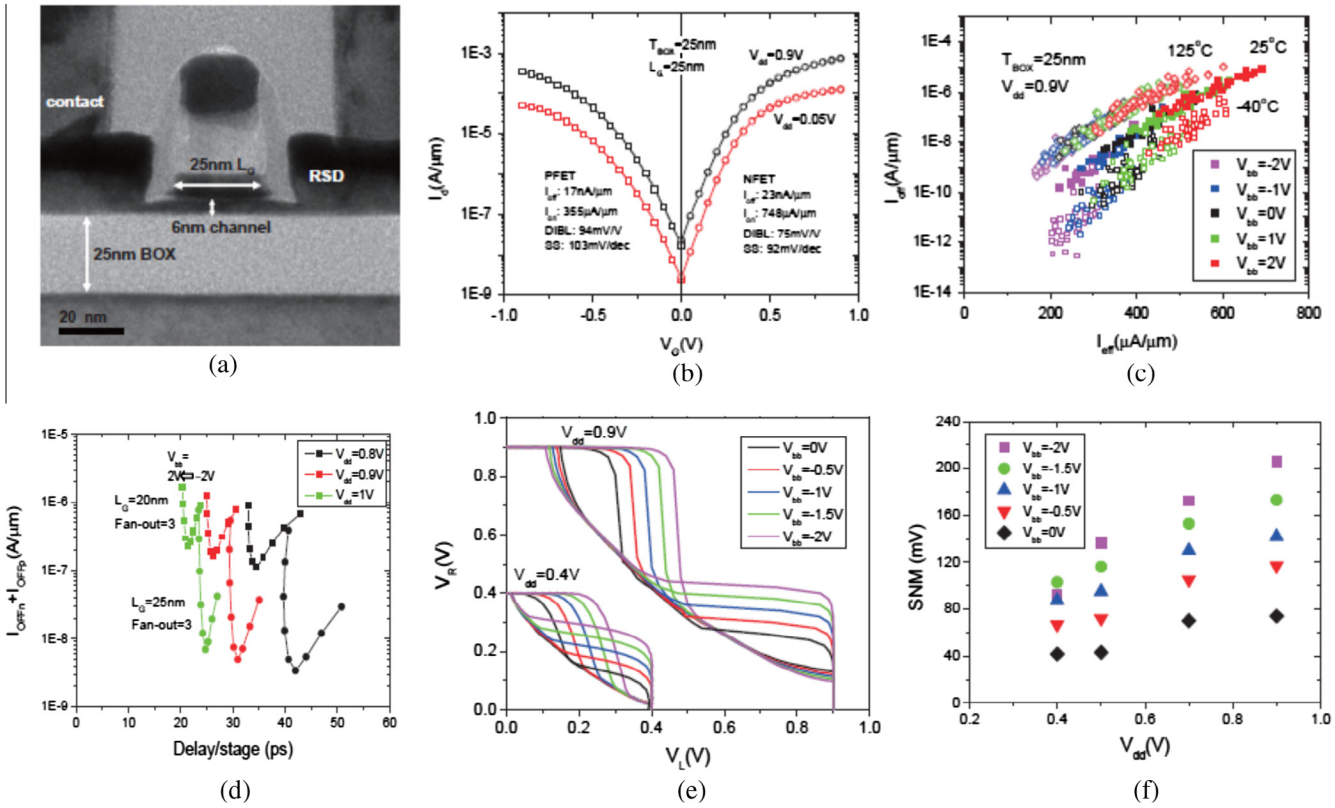


Fig. 8. (a) TEM cross-section of 25 nm BOX UTBB devices with gate length of 25 nm and channel thickness of 6 nm. (b) Id/VG curves of 25 nm BOX UTBB N/PFETs featuring gate length of 25 nm, showing good SCE control. (c) I_{eff}/I_{off} plots of 25 nm BOX UTBB NFETs at −40 °C, 25 °C and 125 °C. Back bias effect is maintained across this wide temperature range. (d) 100 nm CPP ROs delay/stage vs I_{off}, showing clear performance and leakage modulation by back bias. (e) Butterfly curves of the 0.08 µm^2 SRAM, showing clear SNM modulation from back bias. SRAM remains functional down to Vdd 0.4 V. (f) SNM vs. Vdd, showing back bias is very effective to adjust the balance between N/PFETs and achieve higher SNM. After [33].

regular VT (RVT) flavors were demonstrated allowing the-use of IPs already developed in bulk. A significant performance gain was demonstrated. At 1.0 V, RO and SRAM bitcells were 32% and 40% faster at same leakage as compared to Bulk 28 nm. At 0.6 V, FDSOI boost was 84% and 100% respectively. The importance of this work [6] was that it showed the first report of all the 28 nm node technology components integrated onto one chip. These results demonstrated all the basic FDSOI technology elements working together to enable the benefits that the technology has to offer.

In 2012, Arnaud et al. [34] presented the first hardware results for low complexity circuits. This work showed that the dynamic power consumption can be reduced by 90% without any speed degradation by simply selecting the appropriate power supply and body bias couple (Vdd, Vbb) (see Fig. 9). Simulations of a full CPU Core implementation with UTBB showed a total power reduction of −30% and a +40% energy efficiency at identical speed with respect to bulk technology due to back side gate biasing efficiency. This work was a significant step in the realization of 28 nm node UTBB technology with high speed and low power.

The culmination of all the activities and results previously presented enabled the risk production of 28 nm FDSOI [9]. At this time a full 28 nm design platform was made available and the silicon was qualified. FDSOI-based ARM-based chips were shown to operate up to a record frequency of 3 GHz [4,5] using 28 nm UTBB FD-SOI CMOS transistors fabricated in a 7 nm thin layer of silicon sitting over a 25 nm buried oxide (BOX). It was underlined that the process was comparatively simple with respect to FinFET and even conventional bulk technologies. The UTBB FD-SOI was plugged on the basis of the 28LP Bulk HKMG process from ISDA. At this node, more than 10% of the process steps and three masks were saved, resulting in an overall process cost saving of 10% [5]. Only 3 process steps were specific to UTBB FD-SOI, all the others being derived from the conventional 28LP Bulk, namely Raised S/D epitaxy for access resistance reduction; ground plane implantation for threshold voltage adjustment and hybridization for SOI/BULK co-integration.

More recently, other companies demonstrated the interest of 28 nm in products. Sony Corp. revealed that the company's next-generation Global Navigation Satellite System (GNSS) chip will use 28-nm FDSOI process. Moreover, the SFARDS' SF3301 dual-algorithm ASIC chip fully utilizes the advantages of the 28 nm FDSOI technology. With forward body bias, the chip is operational at lower voltage while maintaining a higher frequency. The ASIC's lowest working voltage is 0.45 V.

Finally, it is worth to mention that production of FDSOI technology requires quality compliance and high volume manufacturing readiness of SOI substrates in agreement with the device roadmap. Indeed, this remained for many years a major obstacle to the development of planar FDSOI. Ultra-thin SOI and BOX wafers (UTBOX) for 28 nm FDSOI, where the thicknesses of the target structure are 12 nm silicon and 25 nm BOX to accommodate back bias strategies, had to respect the extremely stringent requirements for thickness uniformity and flatness (critical elements in controlling the threshold voltage variation).

The high volume manufacturing readiness of SOI substrate in compliance with 28 nm FDSOI roadmap was clearly demonstrated in October 2013, when the three main 300 mm SOI manufacturers (SEH, Soitec, and SunEdison) made presentations reporting the achieved film thickness uniformity (see Fig. 10, [3]). Total SOI thickness fluctuations as low as ±0.5 nm were reported.

2.2. From 28 nm to 14 nm FDSOI technology

While the 28 nm node FDSOI technology proved to be a unique opportunity for continued scaling of planar CMOS technology, further shrinking of the technology and additional performance increase posed significant device and manufacturing challenges. We will analyze hereafter the main process innovations proposed and subsequently realized to address these challenges.

Cheng et al. presented a new FDSOI integration scheme in 2009 [35]. The new integration scheme featured implant-free s/d extensions to improve external resistance, zero-Si-loss processing to minimize silicon loss in the s/d region, and faceted in-situ doped RSD to reduce parasitics. All of these new features were integrated into FDSOI devices and were demonstrated to boost performance. The novel s/d epitaxy process was developed to form a *faceted* RSD with in-situ doping (in-situ boron doped – ISBD – SiGe RSD for PMOS and in-situ phosphorus doped – ISPD – Si:C RSD for NMOS). Extensions were created by an RTP anneal to drive dopants in the RSD toward the channel. Compared with conventional vertical RSD epi, the *faceted* RSD epi enabled 15% reduction in total gate to S/D capacitance at constant S/D resistance (Fig. 11). In addition the SiGe:B S/D contact enabled a significant reduction in contact resistivity between the SiGe and the silicide. A cut-off frequency as high as 300 and 260 GHz with such ETSOI NFETs and PFETs (L_g = 25 nm, contacted gate pitch = 260 nm), respectively, were shown in [36,37].

Another primary advantage of this process flow is that S/D and extensions were formed without implantation ("*implant-free*"),

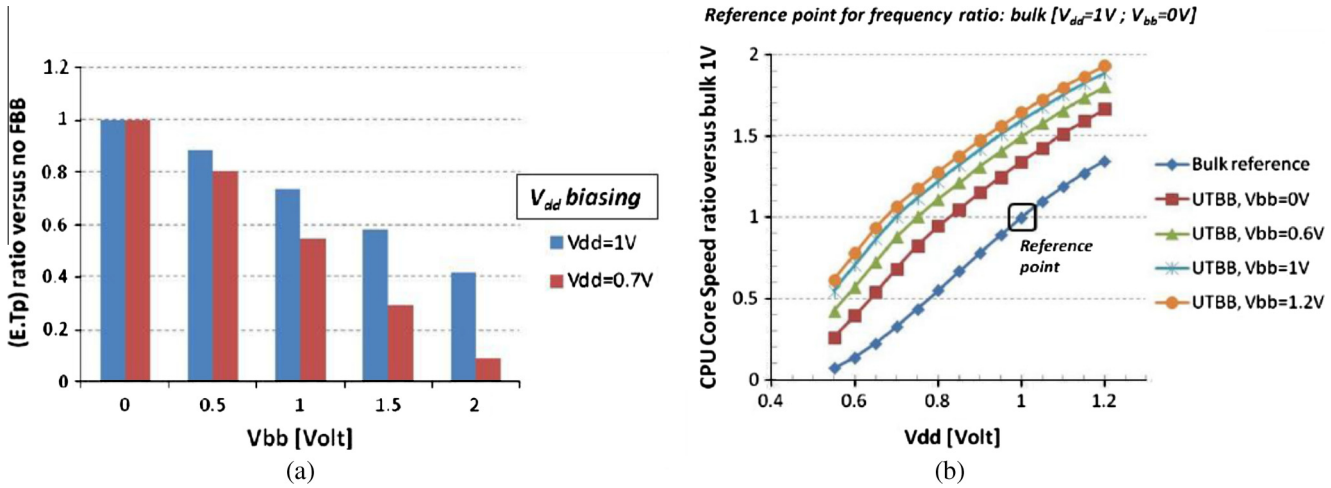


Fig. 9. (a) (Energy·τ_p) product significant improvement with FBB. More than half energy consumption reduction at nominal voltage and up to 8 times decreasing at low voltage [34]. (b) CPU core frequency versus bulk technology. The UTBB architecture brought +30% and forward body bias +30% more compared to bulk (simulated data) [34].

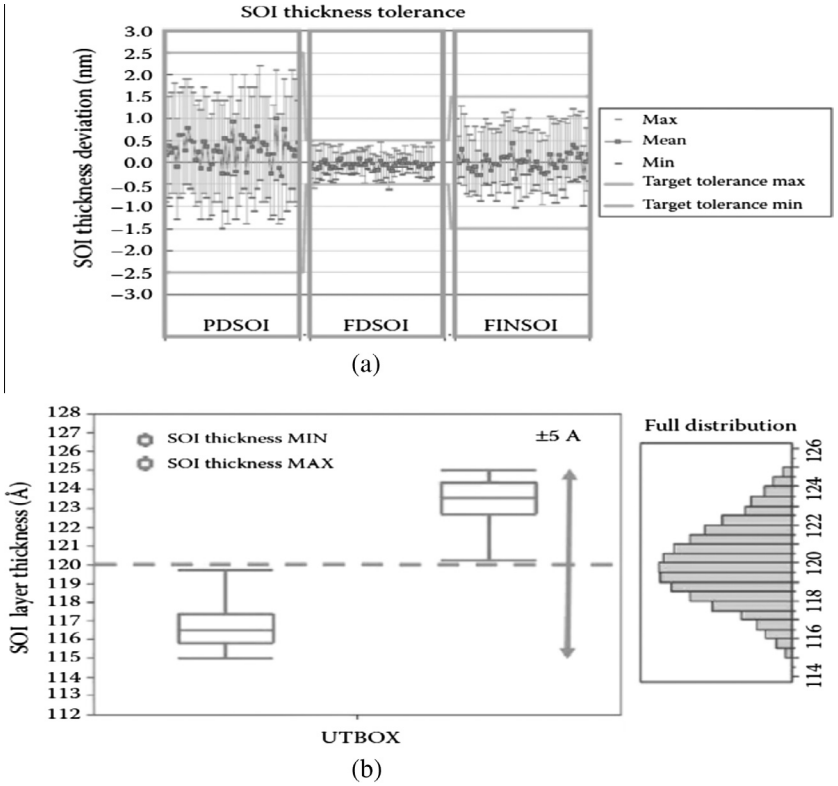


Fig. 10. Top Si film total thickness control of ±0.5 nm as presented by SEH (a) and SOITEC (b) at the SOI technology summit in Shanghai (October 2013). After [3].

therefore eliminating implant-related issues such as ion straggling, amorphization of the thin silicon in the s/d, damaging BOX and segregating dopants into the damaged BOX. The single-crystallinity of the ETSOI layer was maintained during the entire processing. In short channel devices (L_g = 25 nm with T_{Si} = 6 nm and same high-k/MG stack for both NFET and PFET), excellent SCE control was demonstrated, with DIBL less than 100 mV/V and SS less than 90 mV/dec (see Fig. 11). PFET exhibited strong performance of Idsat = 550 μA/μm at I_{off} = 3nA/μm, VDD = 0.9V, and L_g = 25 nm. This result was very impressive even when compared with state-of-the-art bulk LP devices with eSiGe. NFET performance was also among the best FDSOI results reported. Low GIDL (20 pA/μm) and gate leakage (0.5 nA/μm^2) made devices attractive for LP applications. The high drive current of PFETs was attributed to low extension resistance (Rext < 200 Ω μm) by the novel *implant-free* process that eliminated implant-related damages and enabled nearly 100% dopant activation. Fig. 11 shows the improvement in total on-state resistance (Ron) that can be achieved by optimizing the *in situ* SiGe process used to simultaneously form extensions and raised S/D. The new process eliminates several process steps since the S/D and extensions are formed simultaneously.

The work above was extended in [26], where the dual in-situ doped epitaxy for extension and S/D doping was demonstrated in a full CMOS FDSOI integration, moreover supporting multiple gate dielectrics, analog devices and varactors. This work also presented the lowest Vt variation (with AVt = 1.25 mV μm) for the FDSOI devices with undoped channels and in-situ grown extensions, thus eliminating random dopant fluctuation completely. I_{on}–I_{off} curves with drive currents of 640 and 490 μA/μm at I_{off} = 300 pA/μm at VDD = 0.9 V for NFET and PFET, respectively, were achieved, with good short channel control (DIBL < 100 mV/V) and low GIDL at L_g = 25 nm (device dimensions, as gate length, spacer thickness, and contacts were designed so that they fit the targeted pitch of 80 nm). Simulations showed that the successful integration of SiGe and Si:C RSDs provided considerable channel stress and therefore performance improvement. Additional performance gain was achieved by stress transfer from stressed SiN liners and the faceted RSD, as shown in Fig. 11. In fact in FDSOI the conventional *vertical* RSD moves the stressed liner away from the channel thereby hindering stress transfer while the facetted RSD enabled improved stress transfer resulting in 40% increase of hole mobility and 15% enhancement of drive current due to better coupling of stress liner and ETSOI channel.

Research to integrate auxiliary devices directly onto the thin silicon substrate was conducted in 2009–2010 timeframe. Several of the required SOC elements including high voltage devices for I/O and analog devices (passive and active) were reported in [26,36,37]. The implementation of these auxiliary devices directly on the thin silicon layer in the FDSOI logic technology is an alternative to the need of hybrid SOI/bulk integration. In addition, the corresponding circuit design implications were thoroughly assessed.

SOC applications typically require the use of multiple gate dielectrics. Roughly speaking requirements for thin oxide device is T_{inv} = 1.6 nm for logic and thick oxide device and T_{inv} = 4 nm for I/O devices. Since short channel effects in FDSOI are mainly controlled by the channel thickness, thick oxide FDSOI devices can be fabricated showing excellent gate length scaling. Fig. 12 shows the Gm/Gds characteristics of devices with thin and thick oxides as a function of gate length. Significant self-gain is achieved at gate lengths down to 25 nm. For instance, memory access transistors (such as in embedded DRAM) can be scaled to a gate length of about 40 nm resulting in smaller cell size. Also (with exceptional Gm/Gds scaling) medium oxide devices with gate-lengths as small as 35–40 nm can be used for analog applications [37]. The lower Vt of analog devices compared to logic devices was achieved by an optimized spacer process that employed lateral oxygenation to achieve lower Vt for wider NFETs without degrading PFET logic Vt [26].

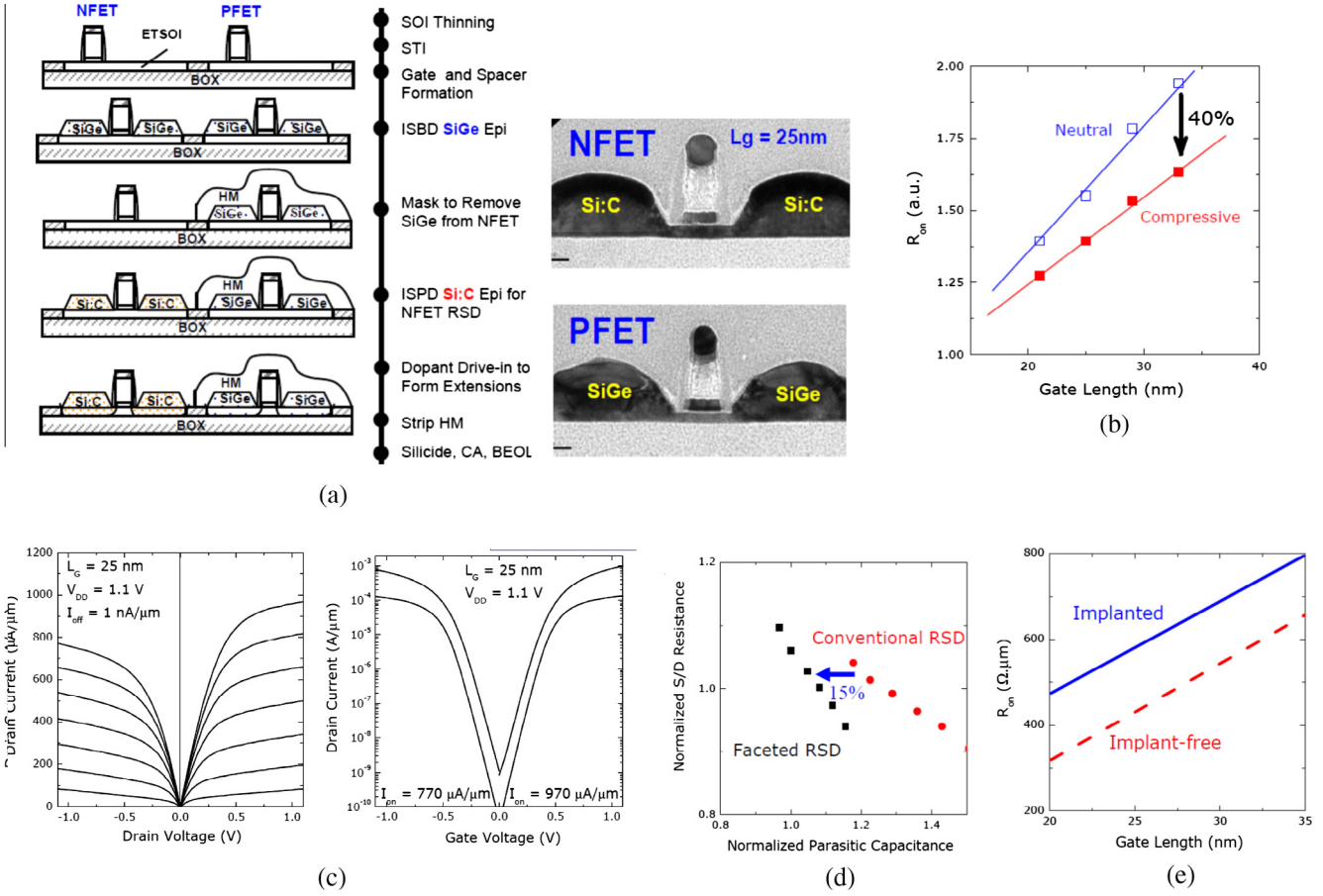


Fig. 11. (a) Novel ETSOI CMOS flow and TEM cross sections showing NFET with ISPD Si:C RSD and PFET with ISBD SiGe RSD [26]. (b) Experimental data demonstrating 40% hole mobility gain from stress liner at 130-nm gate pitch. After [26]. (c) Device characteristics with LG = 25 nm showing excellent subthreshold swing (SS < 90 mV/dec for both NFET and PFET [35]). (d) TCAD simulations showing 15% reduction of parasitic capacitance by faceted RSD at a constant Rext [35]. (e) Ron-LG characteristics of PFET with T_{Si} = 6 nm showing Rext reduction by *implant-free* process [35].

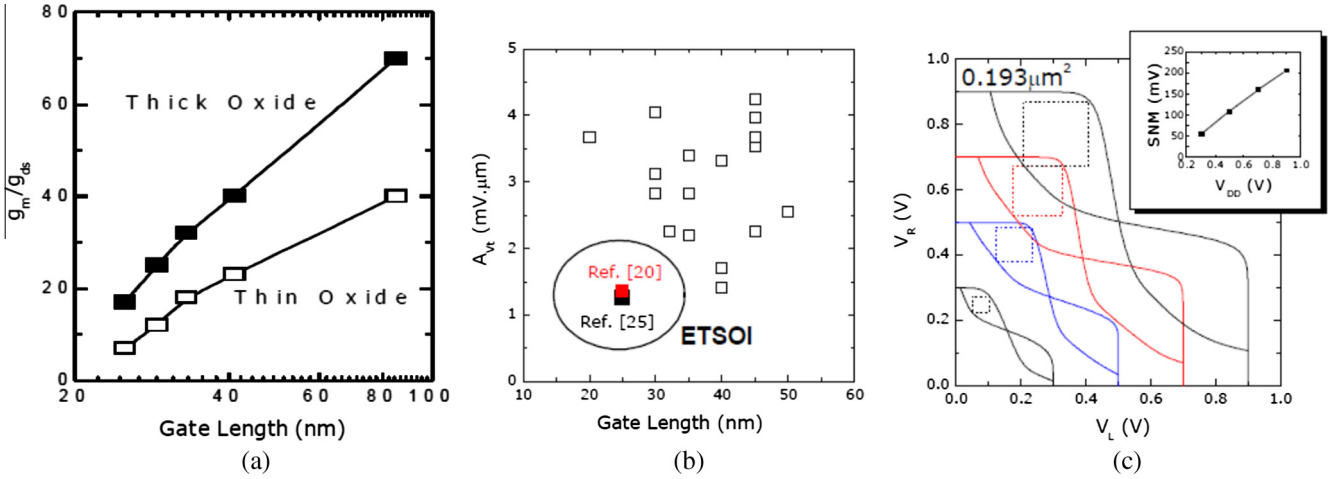


Fig. 12. (a) Excellent analog operation is possible down to LG = 25 nm without the need of special device design or extra well implant [26]. (b) Low Vt variability of ETSOI transistors [37]. (c) SRAM butterfly characteristics demonstrating excellent SNM scaling with supply voltage down to 0.5 V [37].

In [37], it was shown that sub-0.5 V operation of 0.193 μm² SRAM cells were made possible as a result of extremely low Vt variation (A_{Vt} = 1.25 mV μm, with gate length down to 25 nm, see Fig. 12). The record HK/MG device matching, high Gm/Gds scaling to small LG, the absence of history effect in fully-depleted devices, and the need of no additional mask/process step to co-integrate analog blocks with logic ones, suggested FDSOI as a promising solution for next generation general purpose low-power and SoC technologies.

The implant free FDSOI process flow was used as a baseline to further develop and optimize the transistors in 2011 [38,39] when FDSOI CMOS with 22 nm gate length (L_g) and sub-100 nm

contacted gate pitch for system-on-chip (SoC) applications and high density 6-T SRAM cells down to 0.08 μm^2 were demonstrated. 193 nm immersion lithography was used for patterning all critical levels. Advanced high-k/metal gate stacks were engineered to reduce the EOT and to achieve the targeted Vt. The enabled transistors offered competitive drive currents (NMOS/PMOS) of 1150/1050 μA/μm at I_{off} = 100 nA/μm for high performance (HP) and 920/880 μA/μm at I_{off} = 1 nA/μm for low power (LP), respectively, at Vdd = 1 V. The gate height and the raised source drain (RSD) thickness were scaled down to 40 nm and 20 nm, respectively, to reduce the parasitic capacitance between the gate and RSD. Copper damascene local interconnect was adopted to achieve low contact resistance. Fig. 13 shows TEM cross-section of ETSOI transistors with 22 nm L_g, 80 nm gate pitch, 5 nm channel thickness, and 12 nm spacer. Compared with a 28 nm bulk LP technology, the high drive currents of ETSOI transistors coupled with large capacitance reduction by aggressive L_g scaling result in 25% improvement in ETSOI ring oscillator (RO) speed. Auxiliary ETSOI devices including epitaxy resistors with high precision and gated diodes with near ideal characteristics were also fabricated to complete device menu for early FDSOI SoC design.

A long standing concern for FDSOI and for thin body devices in general up to this point had been how to incorporate stress boosters commonly used for the past several generations of conventional bulk and PDSOI technologies. In particular, high performance circuit applications require the use of mobility boosters. In 2012, Khakifirooz et al. and Cheng et al. presented research addressing the high performance requirements [40,41]. Planar FDSOI features carrier transport along the (1 0 0) Si planes. It is well known that electron mobility is highest and hole mobility is lowest for unstrained transport on (1 0 0) surface with ⟨1 1 0⟩ current flow. Thus, the hole mobility gain should be addressed in order to improve the n/p mobility balance. As the efficiency of embedded stressors to transfer the strain in the channel diminishes rapidly for contacted gate pitches (CGP) below 100 nm (due to smaller volume available for external stressors) different mobility booster solutions were proposed, namely contact strain, strained SOI (SSDOI) for NFET, and SiGe-on-Insulator (SGOI) for PFET.

Concerning the contact strain engineering, to replace the stress brought by standard liner technology (facing a serious dilemma as negligible room is left between adjacent gates in future nodes, especially with elongated contact holes), metal contacts were proposed [41], as they constitute a large portion of the pitch in aggressively-scaled technologies and are placed in close proximity to the gate. It was shown that more than 25% increase in PFET performance was achievable by modifying the contact structure. Small degradation in NFET performance was observed with the new contact.

SiGe-on-Insulator (SGOI) as a PFET performance element was also introduced. Two approaches to form SGOI were explored (Fig. 14). In thermal mixing, SiGe was epitaxially grown on PFET regions and Ge diffused into the underlying FDSOI layer by thermal annealing. The SiGe layer was then thinned to the desired thickness. In the condensation technique, after SiGe epitaxy, oxidation was used to preferentially oxidize Si, resulting in SiGe layer with a higher Ge concentration. The oxide layer was then removed. Low-temperature epitaxy pre-clean was critical to avoid agglomeration of SiGe channel and strain loss. High resolution XRD analysis demonstrated that the SGOI layer remains fully strained during device processing. Fig. 14 shows the TEM cross-section of the SiGe channel ETSOI device with 6-nm channel thickness and 23% Ge content. As shown in Fig. 14, roughly 35% increase in device performance is demonstrated in 23% SGOI devices compared to SOI Si channel control.

A breakthrough in mobility enhancement for pMOS was presented by Cheng et al. in 2012 [40]. This work demonstrated the first high performance hybrid channel ETSOI CMOS by integrating strained SiGe-channel (cSiGe) PFET with Si-channel NFET at 22 nm ground-rules. An "STI-last" integration approach to achieve thin and uniform SiGe channel (to maintain good short-channel control and low variability in devices with various widths) was also introduced. In the conventional approach ("STI-first") SiGe is epitaxially grown after shallow trench isolation (STI). This leads to a non-uniform SiGe channel due to the faceted SiGe epitaxy at the edge of the active areas. In the new integration scheme the SiGe was first grown as a blanket film across the entire wafer and then removed from NFET regions by a SiGe etch process highly selective to Si. The SiGe/Si bilayer in PFET region was then converted into a single SiGe layer by a condensation process consisting of a high temperature oxidation process which oxidizes the Si in the SiGe layer while pushing the Ge downwards into the underlying thin Si layer. The new scheme not only produced uniform SiGe channel but also enabled enhanced drive current (Iod_{lin}) even when the device width was reduced to 40 nm. The device performance enhancement was due to the conversion of biaxial stress in wide devices to uniaxial stress in narrow devices, as described later. Both nano-beam diffraction (NBD) and X-ray diffraction (XRD) further confirmed that SiGe layer was compressively strained after epitaxy and compressive strain was fully retained after thermal condensation.

In-situ phosphorus doped (ISPD) Si:C and *in-situ* boron doped (ISBD) SiGe were grown as RSD of NFET and PFET, respectively. Extensions were formed by driving the dopants from RSD toward the channel without the need of ion implantation. TEM and EDX maps in Fig. 15 show a PFET with 6 nm SiGe channel, 22 nm gate length, 100 nm contacted gate pitch (CGP), and ISBD SiGe RSD. It

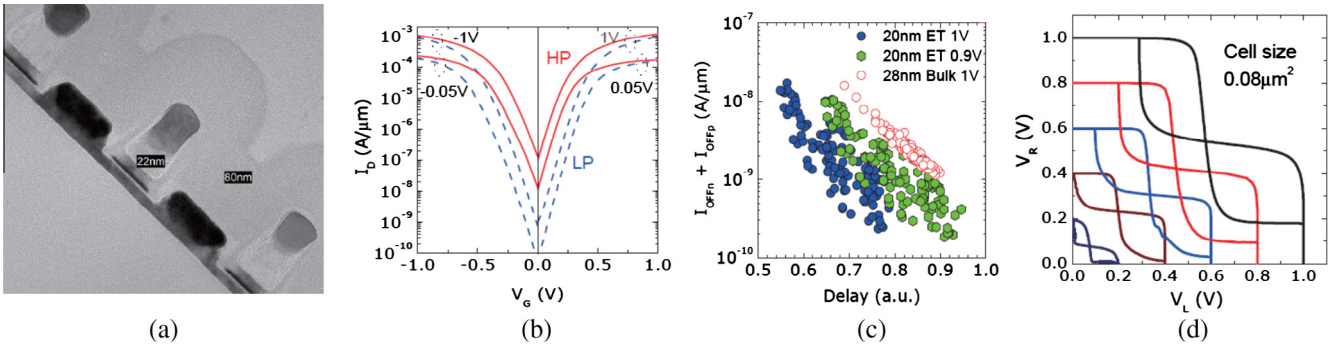


Fig. 13. After [38]. (a) TEM shows ETSOI transistor with 22 nm LG, 5 nm T_{Si}, 12 nm spacer and 80 nm gate pitch. (b) Transfer characteristics of HP and LP ETSOI devices. (c) ETSOI RO benchmark with respect to 28 nm bulk LP shows 25% improvement in speed at the same voltage, or 20% VDD reduction at the same speed. (d) Butterfly curves of a 0.08 μm^2 ETSOI SRAM cell down to 0.2 V VDD.

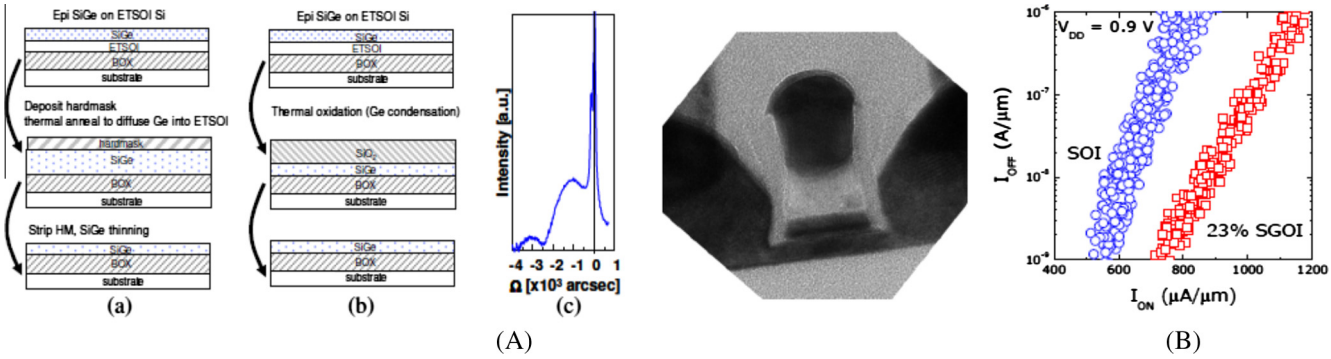


Fig. 14. (A) Left: Schematic process flow to form SiGe-channel ETSOI (a) thermal mixing, (b) condensation, (c) HRXRD data showing compressively strained SGOI with 23% of Ge. Right: TEM cross-section of SiGe channel ETSOI with a channel thickness of 6 nm. After [41]. (B) PFET I_{ON}–I_{OFF} characteristics demonstrating 35% increase in the performance by using 23% SGOI channel. After [41].

was shown that the SiGe channel formed by thermal condensation (25% Ge) did not introduce additional variability (as evidenced by the matching Vt distributions between SiGe channel and Si control). The robustness of the hybrid channel CMOS integration flow was further evidenced by good pattern fidelity in a highly scaled SRAM array and demonstration of functional 0.08 μm^2 SRAM fly-cell with Si NFETs and SiGe PFETs (Fig. 15).

The crucial role of compressive channel strain and more desirable longitudinal uniaxial strain (strain parallel to the current flow direction) to achieve high performance SiGe PFET was thoroughly examined and presented. In fact, while strain relaxation *parallel* to the channel direction has adverse impact on device performance, one can exploit strain relaxation *perpendicular* to channel direction to improve device performance. Fig. 15 shows that biaxial compressive strain in wide SiGe-channel PFETs results in 26% improvement in *effective* drive current (I_{eff}) compared to Si devices, I_{eff} being defined as:

$$I_{eff} = 1/2\ (I_{high} + I_{low}) \quad (1)$$

wherein I_{high} = Ids (Vgs = Vdd and Vds = ½ Vdd) and I_{low} = Ids (Vgs = ½ Vdd and Vds = Vdd).

Uniaxial stress in narrow width SiGe PFETs enabled further performance improvement as evidenced by the higher drive current (Iodsat) as the device width (W) decreases (Fig. 15). For unstrained Si channel, Iodsat was independent of W. Unlike embedded SiGe (eSiGe) source/drain which degrades with CGP, channel SiGe (cSiGe) produces strain directly in the channel independent of CGP. Therefore, cSiGe strain remains effective from node to node. Besides improving device performance, it was underlined that another advantage of using SiGe channel relies on the fact that SiGe modulates device Vt as evidenced by the C–V characteristics in Fig. 15. Such a Vt modulation by SiGe channel provided an additional knob to achieve multi-Vt. Si channel NFET and PFET were used for SRAM devices to maintain ultra-low leakage current including low gate-induced drain-leakage (GIDL). All device channels advantageously remain undoped to eliminate random doping fluctuation thereby reducing device variability. A drawback of SiGe PFET compared with Si PFET is the increase of GIDL current in SiGe PFET due to the smaller band gap of SiGe and thus enhanced band-to-band tunneling. However, the total off current of SiGe PFET was still well below the leakage current limits of most high performance and low power logic devices.

Many of the process innovations and performance boosters were further developed and implemented using the thin BOX substrate platform. In 2013, Liu et al. [42] presented high performance Ultra-thin Body and BOX (UTBB) FDSOI devices with a channel thickness of 6 nm, BOX thicknesses (T_{BOX}) of 25 nm and gate length (L_G) of 20 nm, featuring dual channel FETs (Si channel NFET and strained SiGe channel PFET) (Fig. 16). The simplified UTBB integration flow is shown in Fig. 16. The PFET cSiGe channel used in this study was formed by epitaxy & condensation. A thin SiN liner was deposited inside the trench cavity to reduce the risk of epitaxial S/D shorting to the substrate. After high-k/metal gate formation, a dual in-situ doped RSD process was followed to form NFET and PFET. Here, the NFET RSD was Phosphorus doped Si:C, and PFET RSD was Boron doped SiGe. Both doping levels were >5 × 10^{20} cm^{-3} to achieve low external resistance (Rext). A combination of laser annealing & RTA was applied to fully activate the dopants and minimize Rext. Conventional MOL and BEOL process steps completed the device fabrication. Competitive effective current (I_{eff}) reaching 630 μA/μm and 670 μA/μm for NFET and PFET, respectively, at I_{off} of 100 nA/μm and V_{dd} of 0.9 V were reported.

Excellent electrostatics was shown, demonstrating the scalability of these devices to 14 nm and beyond. Very low AVt (1.3 mV μm) of channel SiGe (cSiGe) PFET devices was also reported for the first time. BTI was improved >20% vs a comparable bulk device & evidence of continued scalability beyond 14 nm was provided. The significance of this work was that it was the first demonstration of all the key enabling features including dual *in-situ* doping and SGOI channel on a UTBB platform. The technology features presented in Liu's work from 2013 [42] were used as the basis to establish the process flow for the 14 nm node UTBB technology.

In 2014, Weber et al. [43,44] presented the 14 nm device platform designed for high speed and energy efficient applications using strain-engineered FDSOI transistors (Fig. 17). All the new front-end process elements were demonstrated including dual SOI/SiGeOI N/P channel, dual workfunction gate-first HKMG integration scheme and a dual in-situ doped Si:CP/SiGeB N/P raised source-drain. Fig. 17 highlights these module changes in the process flow as well as the key 14 nm FDSOI design rules and technology features. Starting from an Ultra-Thin Body and Buried oxide (UTBB) SOI substrate, the strained-SiGe channel (cSiGe) was selectively formed in PMOS areas by SiGe epitaxy growth followed by a Ge condensation. The SiGe channel has been introduced to boost the hole mobility and to lower the threshold voltage (Vt) for PMOSFETs. The cSiGe process was realized before STI patterning to avoid SiGeOI over-thinning linked to the Ge condensation process at active edges. As shown in Fig. 17, channel strain has been experimentally measured by Nano-Beam electron Diffraction (NBD) at the end of the process: 1% compressive strain in the 6 nm thin SiGeOI channel was demonstrated, corresponding to a fully-strained Si0.75Ge0.25 channel. After the cSiGe integration, hybrid bulk areas were formed by etching away the BOX in specific designed areas, providing a space for passive devices and ESD FETs to be built. The 14 nm Node device suite is presented in the table of

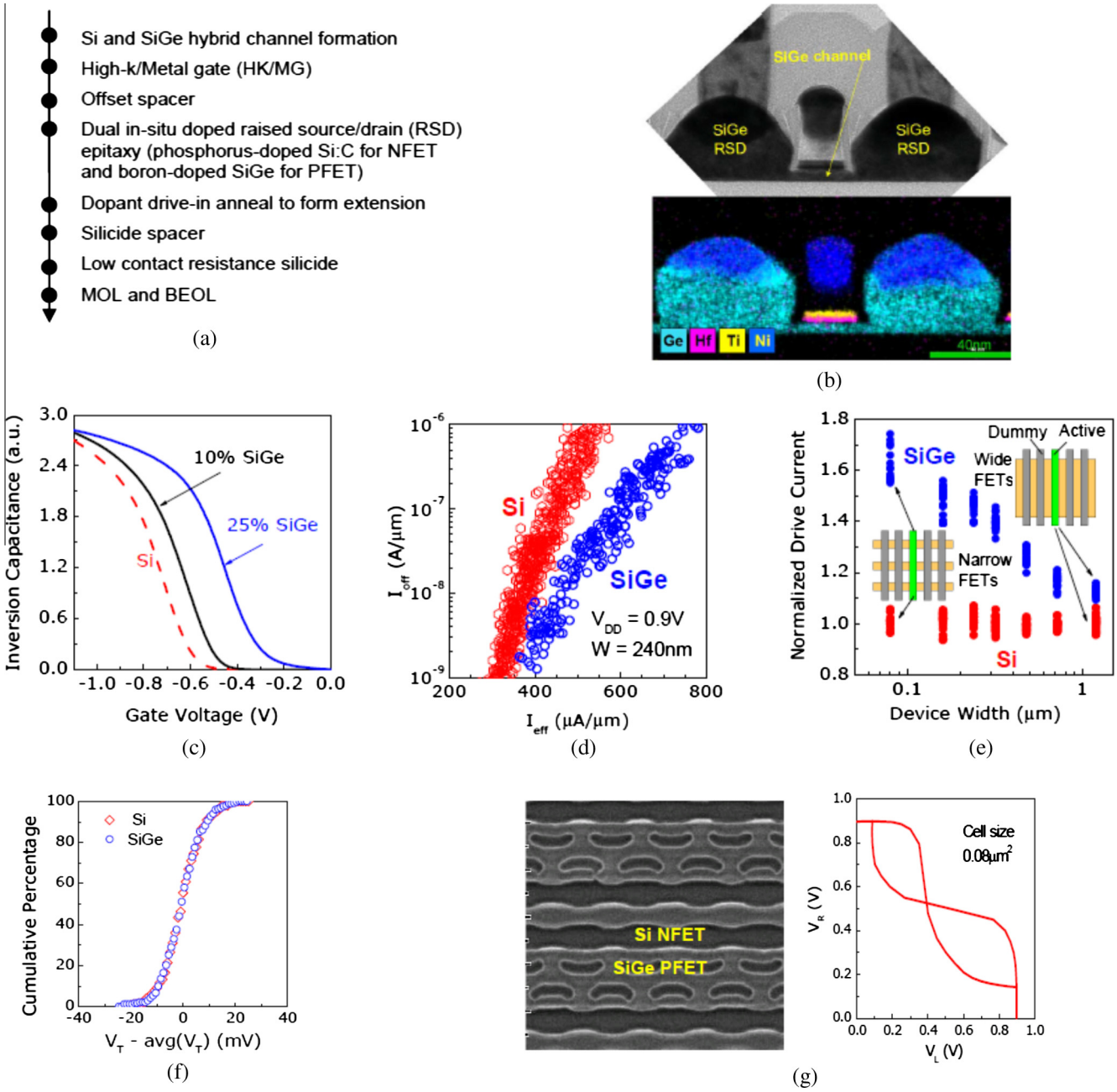


Fig. 15. After [40]. (a) Process flow for fabricating ETSOI CMOS with hybrid Si and SiGe channels, gate first HK/MG, and dual in-situ doped RSD. (b) STEM and EDX map showing a SiGe channel PFET with 6 nm channel thickness, 22 nm Lgate, 100 nm contacted gate pitch, HK/MG, and ISBD SiGe RSD. (c) C–V plot showing multi-Vt PFETs can be obtained by Si and SiGe channels with the same gate stack. (d) PFET I_{eff}–I_{off} plot showing ETSOI SiGe PFET with I_{eff} = 615 μA/μm at I_{off} = 100 nA/μm and VDD = 0.9 V. Device width is 240 nm. Narrow SiGe PFETs have even higher I_{eff}. (e) PFET drive current (Iodsat) vs. device width (W). For Si channel, Iodsat is independent of W. For SiGe channel, Iodsat increases as W decreases, indicating further performance enhancement in narrow width SiGe PFET. (f) Comparison of PFET Vt variation of SiGe channel vs. Si channel indicating that SiGe (25% Ge) does not introduce additional variability. (g) Left: Topdown SEM of a 0.08 μm^2 6-T SRAM array after formation of SiGe in PFET region and Si in NFET region. Right: Butterfly curves of a 0.08 μm^2 ETSOI SRAM flycell with Si NFETs and SiGe PFETs, demonstrating the cSiGe patterning fidelity with tight ground rules.

Fig. 17. Next, the dual work-function high-k metal gate stack featuring a gate-first approach was fabricated by stack deposition and patterning. After gate patterning, a dual raised source–drain integration was performed. A first nitride film was deposited. The spacer and the in-situ doped SiC:P epitaxy were then selectively formed in NMOS areas. Next, a second nitride layer was deposited for NMOS protection, followed by the PMOS spacer and the in-situ doped SiGe:B formation. The NMOS spacer was constituted by the first nitride material, while the PMOS spacer was made of the first and the second nitride bilayer.

Fig. 17 shows NMOS and PMOS nominal transistors with Si:CP and SiGe:B raised source–drain, respectively. Since gate-to-drain capacitance (Cgd) is of high importance in the total front-end parasitic capacitance and thus for circuit speed, spacer, poly thickness and raised source–drain epitaxy have been optimally designed to minimize Cgd while maximizing the DC transistor performance. Id–Vg plots at Vdd = 0.8 V supply voltage for L = 20 nm and L = 30 nm are presented in Fig. 18. Transistors showed a DIBL of 85 mV and a sub-threshold slope of 85 mV/dec. for both NMOS and PMOS at Lnom = 20 nm. The gate length increase from 20 nm

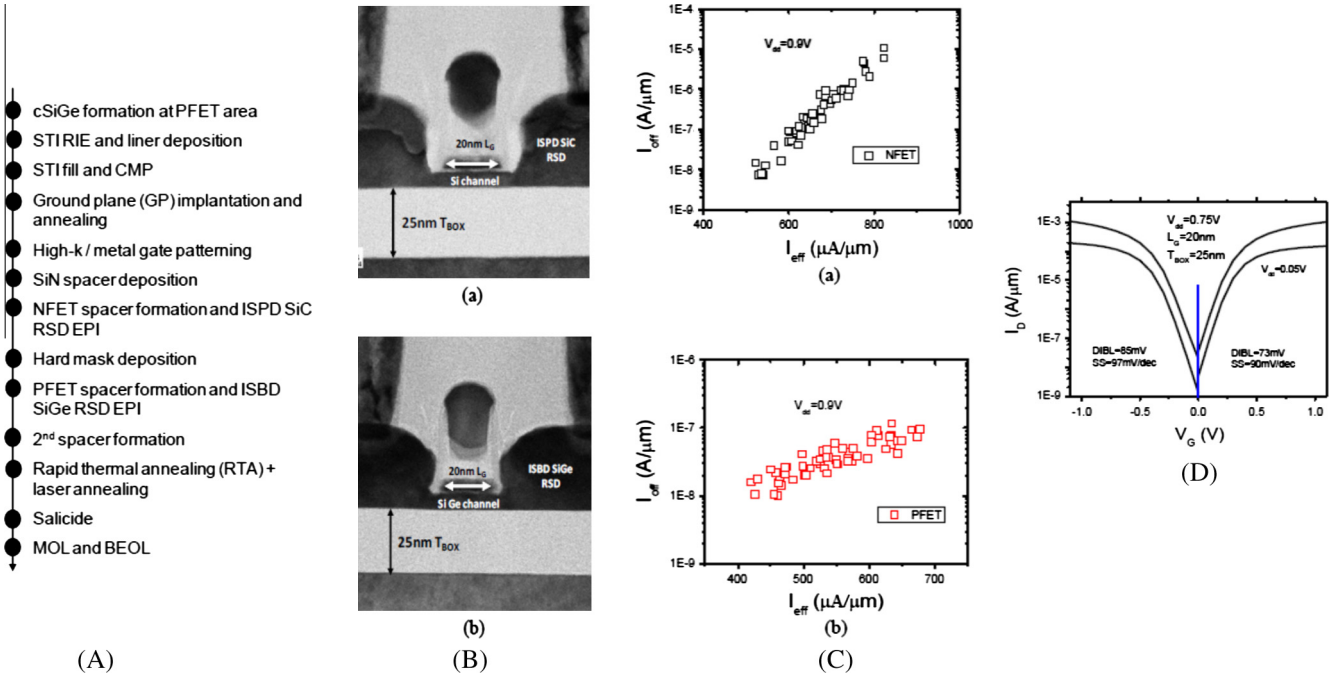


Fig. 16. After [42]. (A) A simplified UTBB FDSOI integration flow, featuring cSiGe PFET, gate first high-k/metal gate and dual in-situ doped raised source/drain epitaxy process. (B) TEM cross-section of (a) NFET with Si channel and in-situ P doped (ISPD) Si:C RSD and (b) PFET with SiGe channel and ISBD SiGe RSD, with gate length of 20 nm and Box thickness of 25 nm. (C) At Vdd = 0.9 V, and an off current of 100 nA/μm, (a) NFET effective current is 630 μA/μm, while (b) PFET effective current reaches 670 μA/μm. The slope of PFET I_{eff}/I_{off} differs from NFET, due to the strain in the cSiGe channel. (D) ID/VG curves of N/PFET with LG at 20 nm, and Vdd at 0.75 V, again, showing excellent electrostatic.

up to 30 nm in the same 90 nm contacted poly pitch (CPP) allowed to reduce the off-leakage by more than 1 decade. Id–Vd plots Idsat = 880 μA/μm & 900 μA/μm at I_{off} = 100nA/μm and Vdd = 0.8V were achieved at Lnom = 20 nm/Wnom = 0.17 μm for NMOS and PMOS respectively. As a result of low Cgd and large PMOS drive current, 14 nm FDSOI technology demonstrated a −34% delay gain with the Fan-Out 3 (FO3) RO inverters at the same static leakage and a −100 mV Vdd reduction (0.8 V vs 0.9 V) over the 28 nm FDSOI.

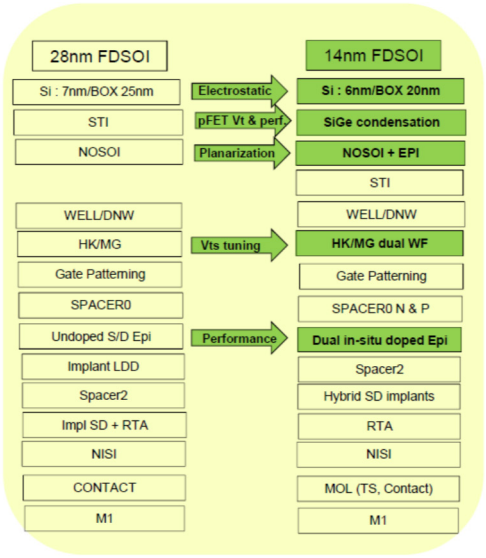
The results clearly demonstrate >50% speed frequency in 14FDSOI at 0.8 V Vdd vs 28FDSOI at 0.9 V Vdd. The importance of this data is that 14 nm FDSOI can run as fast as 28 nm FDSOI with supply voltage much lower than Vdd = 0.8 V, and thus with much lower dynamic power consumption. Compared to the 28 nm FDSOI technology, the so-proposed 14 nm FDSOI technology provided 0.55× area scaling (due to the introduction of local interconnect and the adoption of fixed layout shapes (or "constructs") and delivered a 30% speed boost at the same power, or a 55% power reduction at the same speed, due to an increase in drive current and low gate-to-drain capacitance [43] (see Fig. 18). Using forward back bias (FBB) it was experimentally demonstrated that the power efficiency of this technology provided an additional 40% dynamic power reduction for ring oscillators working at the same speed. Finally, a full single-port SRAM offering was reported, including a 0.081 μm^2 high-density bitcell and two 0.090 μm^2 bitcell flavors used to address high performance and low leakage-low V_{min} requirements.

The 14 nm node FDSOI technology platform was further improved and recently, in 2015 Weber et al. [45] reported a 17% faster delay per stage at the same leakage. It was shown that the same AC performance of 28 nm node FDSOI technology at a 0.9 V supply voltage can be reached at 0.6 V in 14 nm FDSOI technology. This corresponds to a 50% increase in frequency at the same dynamic power, or a 65% power saving at the same operation frequency. The transistors were optimized to provide better drive current and, for the first time, a SiBCN low-k spacer material was integrated in a gate-first FDSOI technology, providing a 10% reduction in gate-to-source/drain parasitic capacitance. The dual raised source–drain integration is illustrated in Fig. 19. After gate patterning, a 6 nm SiBCN ALD film was deposited. The NMOS spacer and the in-situ doped SiC:P epitaxy were then formed. Next, a SiN layer was deposited (either 3 or 4 nm) for NMOS protection, followed by the PMOS spacer and the in-situ doped SiGe:B formation. The NMOS spacer was fabricated using the 6 nm SiBCN material, while the PMOS spacer was made of a 6 nm SiBCN and a 3–4 nm SiN bilayer.

PMOS I_{eff}/I_{off} performance was enhanced by a few % with SiBCN. SiBCN reduced the PMOS ON-resistance (RON) by 10% in addition to the expected gain on the gate-to-S/D fringe capacitance associated with the low-k spacer material. The PMOS R_{ON} and the I_{eff}/I_{off} performance were further improved by a reduction of the SiN layer from 4 to 3 nm, due to a better junction overlap. On the other hand, NMOS performance remained mostly unchanged with SiBCN. Record-low AVt mismatch factors of 1.2 mV μm were reported in Fig. 19 for both N&PMOS with SiBCN, similar to those of the SiN spacer reference. Finally, the AC benefit of the low-k spacer integration was demonstrated. The change of NMOS spacer material from SiN to SiBCN provides a 10% reduction in N + P gate-to-drain capacitance (Cgd), leading to an improved effective load capacitance (Ceff) (−6%) in fan-out-3 (FO3) ring oscillators (ROs). Combining DC and AC benefits, devices with the spacer SiBCN6 + SiN3 demonstrated a 10% faster delay per stage at the same static leakage when compared to the SiN6 + SiN4 reference (Fig. 19).

2.3. Beyond the 14 nm FDSOI technology

While there have been concerns regarding the scalability of FDSOI beyond 14 nm node, we will show several options that enable further scaling (to the 10 nm node and beyond) with enhanced performance. Electrostatics can be improved by scaling

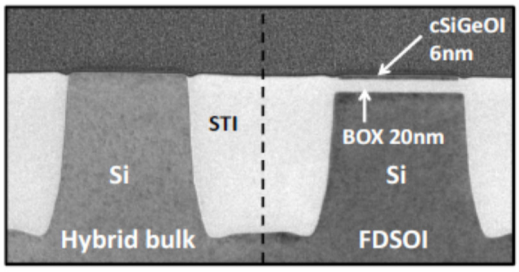


Key features	28FDSOI	14FDSOI
Min CPP	114nm	90nm
M1 pitch	90nm	64nm
Std cell area	1X	0.55X
VT flavours	RVT / LVT	LVT / SLVT
Lgate in min CPP	24, 26, 28, 30nm	24, 26, 28, 30, 32, 34nm
Channel thickness	7nm	6nm
BOX thickness	25nm	20nm

(a)

Key features	28FDSOI	14FDSOI
Min Contacted gate pitch CPP	114nm	90nm
M1 pitch	90nm	64nm
Std cell area	1X	0.55X
VT flavours	RVT / LVT	LVT / SLVT
Lgate in min CPP	24nm → 30nm	20nm → 34nm
Channel	SOI 7nm	Dual SOI/SiGeOI 6nm
Buried oxide	BOX 25nm	BOX 20nm
Gate	HKMG single metal	HKMG dual WF
Source-Drain	Single Si epi + I/I	Dual epi SiGeB/Si:CP

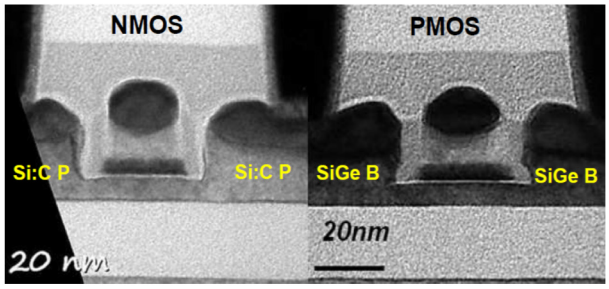
(b)



(c)

Device offer	FDSOI	Hybrid
Digital	X	
I/O & Analog	X	
Memory	X	
ESD	X	X
Varactors	X	X
Resistors	X	X
Bipolars, Diodes		X

(d)



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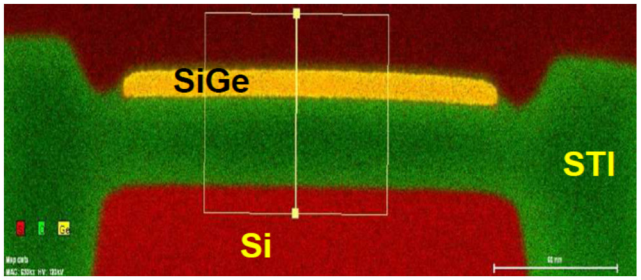

(f)

Fig. 17. After [43,44]. (a) Process flow sequence in 14 nm FDSOI compared to 28 nm FDSOI, with most important module changes highlighted in green and table with key technology features. (b) Key 14 FDSOI ground rules and technology features. (c) TEM picture before HK deposition, illustrating the cSiGeOI pMOS area and the SOI/Bulk flat transition. (d) 14 FDSOI device offer: SOI vs Hybrid bulk. (e) TEM pictures of NMOS and PMOS nominal transistors. (f) Energy dispersive X-ray (EDX) – TEM picture of the strained-SiGe On Insulator (SiGeOI) channel after STI formation.

the T_{Si} and the BOX thickness. Performance can be enhanced by applying effective strain techniques (both in PFET and NFET), and considering layout optimization. It is worth to mention that FDSOI technology offers the advantage of sustaining significant stress within the channel without plastic relaxation (the thin channel staying below the critical thickness [46]). In this section, we will review the new processes and scaling enablers recently explored in the literature to scale FDSOI beyond 14 nm.

One approach to maintain electrostatic control as the gate scales down is to reduce the channel thickness. To this end, several studies in the literature proved the feasibility and manufacturability of extremely thin SOI film and thin BOX for the most advanced FDSOI technology nodes. In [47], the scalability of both unstrained and strained FDSOI CMOSFETs (with single Si-channel) was experimentally demonstrated down to 2.5 nm film thickness and 18 nm gate length with HfO_2/TiN gate stack (see Fig. 20). Off-state currents in the pA/μm range were achieved for 18 nm short and 3.8 nm thin MOSFETs thanks to outstanding electrostatic control, with 67 mV/dec subthreshold swing and 60 mV/V DIBL. For such thin bodies, strain induced Ion gain as high as 40% was demonstrated on the shortest transistors. Long channel transistors mobility for various film thicknesses was also extracted. It was shown that while hole mobility in Silicon was not impacted by the strain in the strong inversion regime, n-sSOI devices revealed larger

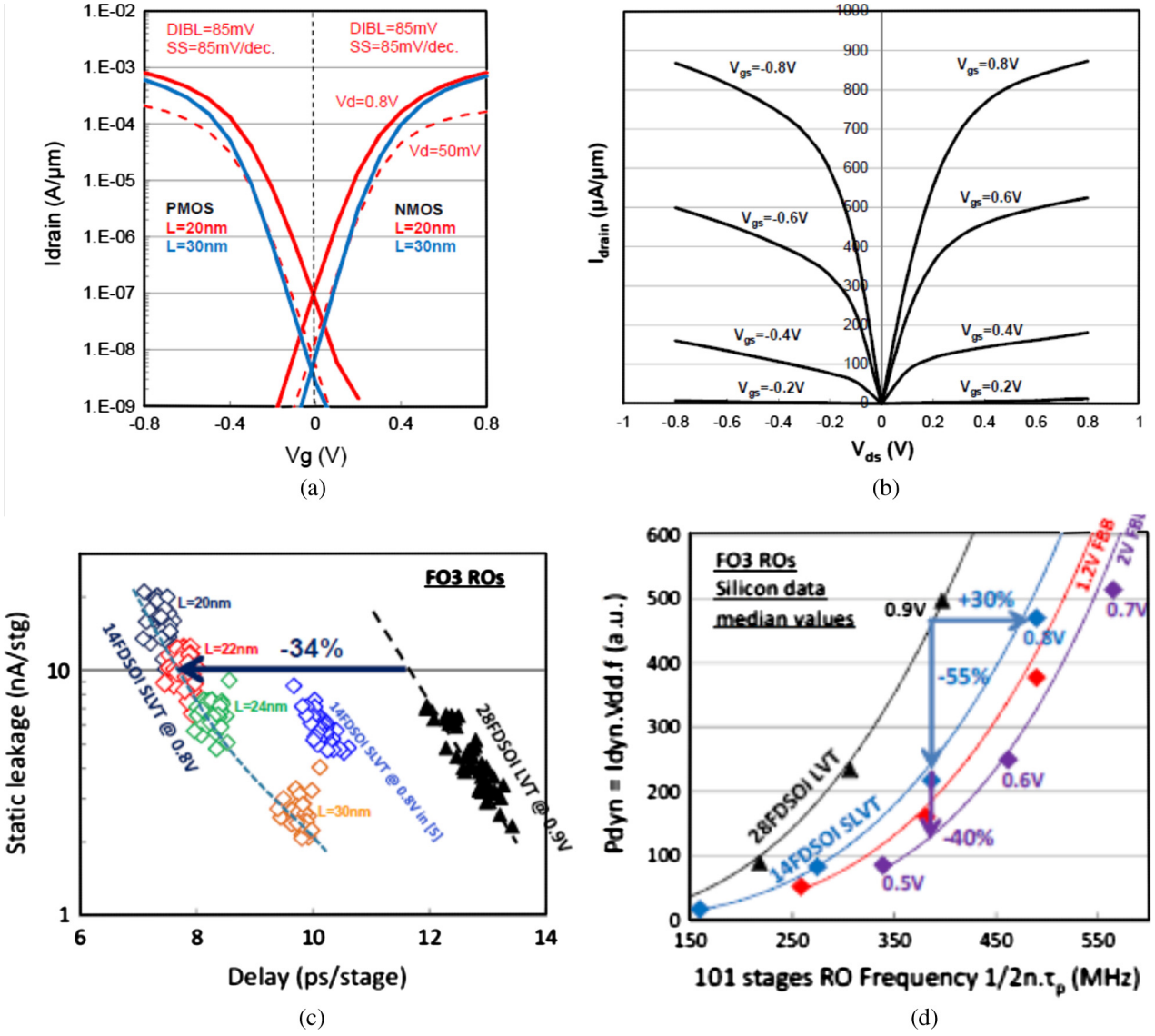

Fig. 18. After [43,44]. (a) Id–Vg plots for Lnom = 20 nm and L = 30 nm and (b) Id–Vd plot at Lnom = 20 nm for both NMOS and PMOS transistors. (c) Delay/Isat in FO3 ring oscillators in 14 nm FDSOI technology at Vdd = 0.8 V compared to the 28 nm FDSOI technology at Vdd = 0.9 V. (d) RO frequency vs Pdyn for various Vdd and various FBB up to 2V.

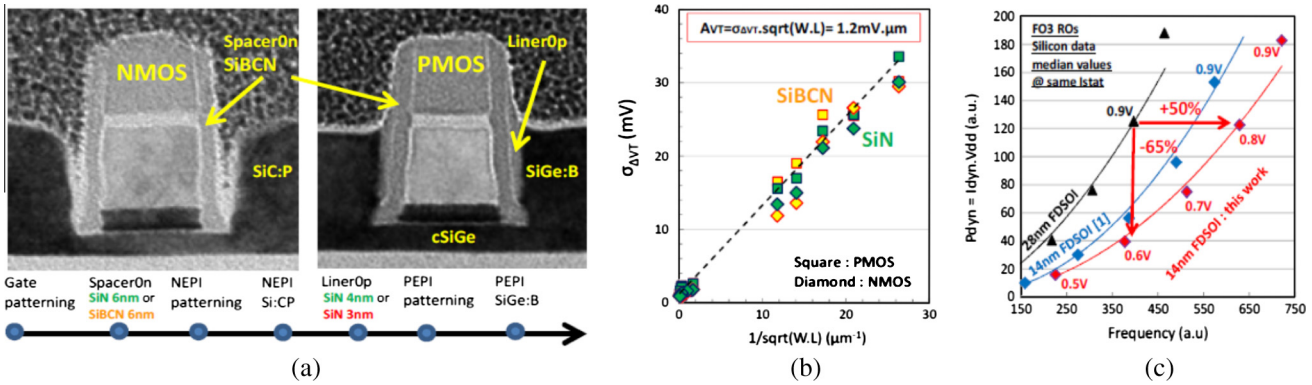

Fig. 19. After [45]. (a) Dual-Epi process flow sequence with low-k SiBCN spacer0n insertion. (b) Vt mismatch for N and PMOS with SiBCN vs SiN as spaceron. (c) Frequency vs. Pdyn demonstrating −65% power vs. 28 nm FDSOI at the same speed.

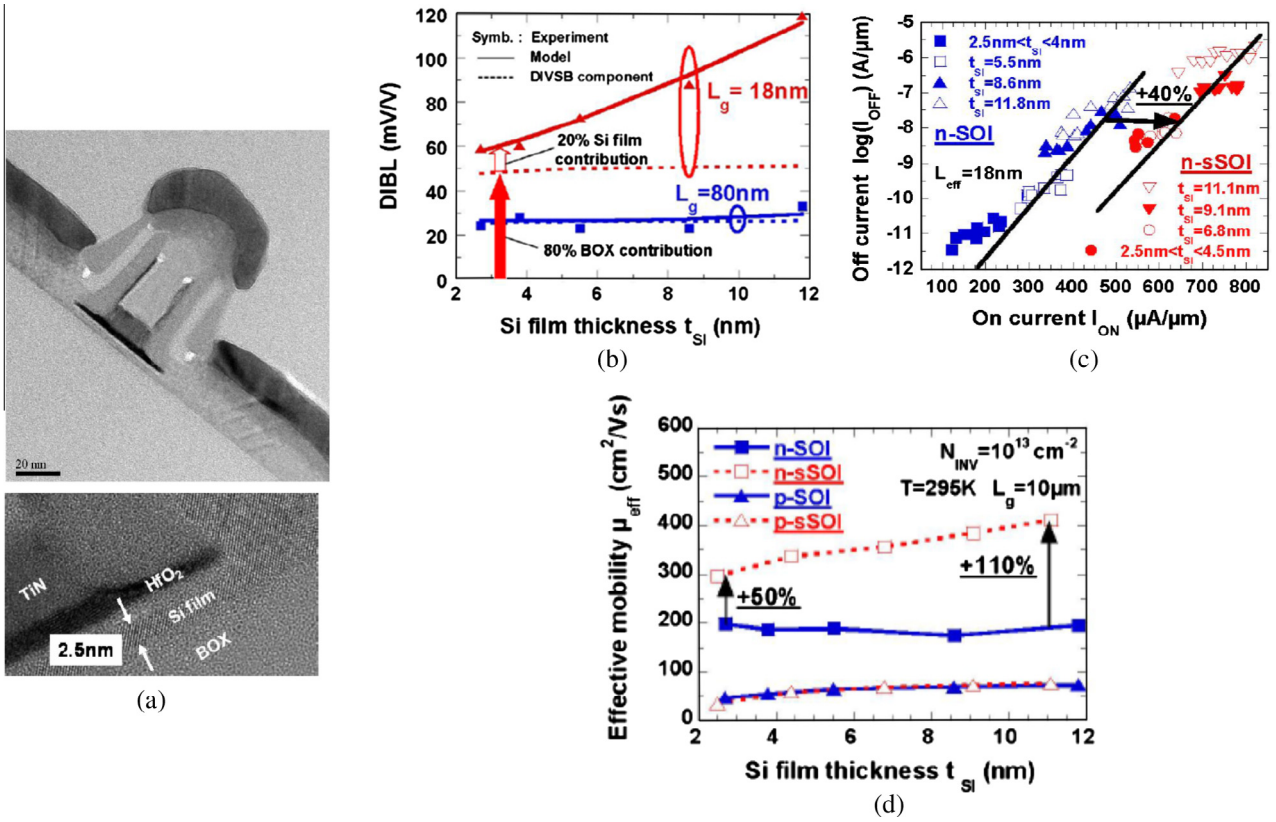

Fig. 20. After [47]. (a) Up: TEM cross-section of 18 nm gate-length n-sSOI MOSFET. Down: HRTEM cross-section showing the detail of the channel edge. The Si film thickness is 2.5 nm. (b) DIBL as a function of the Si film thickness. Fringe fields component can represent 100% of DIBL for LG = 80 nm and up to 80% for LG = 18 nm. (c) I_{off} (Ion) results obtained on 18 nm gate length n-SOI and n-sSOI transistors for various film thicknesses. A performance gain of about 40% is achieved thanks to strain at a given I_{off}. (d) Long channel electron and hole mobilities in high inversion regime. Up to 110% gain is achieved for the thickest (11.8 nm) devices, whereas 50% is obtained for the thinnest (2.5 nm).

electron mobility values with a mobility gain ranging from 110% for the thickest higher films (11 nm) to 50% for the thinnest (<3 nm), demonstrating strain conservation down to T_{Si} = 2.5 nm.

Khakifirooz et al. [48] reported high-performance extremely thin SOI MOSFETs fabricated with a channel thickness down to 3.5 nm, sub-20-nm gate length, and contacted gate pitch of 100 nm. Here the buried oxide (BOX) thickness was of 145 nm. Fig. 21 shows a high-resolution cross-sectional TEM of the FDSOI MOSFET with a channel thickness of 3.5 nm, showing also that faceted RSD structure was successfully formed owing to the low-temperature epitaxy process. At an effective channel length of 18 nm, a drain-induced barrier lowering of 100 mV was achieved by either thinning the channel to 3.5 nm or by applying a reverse back-gate bias to the 6 nm channel MOSFETs. Note that the ability to increase carrier confinement with a back-gate bias is unique to FDSOI and is not available in other device architectures.

Moreover, due to the implant-free process used for *in situ* doped RSD, no increase in series resistance was seen when the channel was scaled to 3.5 nm, resulting in no performance degradation with SOI thickness scaling. No mobility dependence on channel thickness was seen. Finally, Fig. 21 also shows the effective current (I_{eff}) and saturation current (Ion) as a function of the off-current of the FDSOI devices. At an off-current of 100 nA/µm and at Vdd = 0.9 V, I_{eff} and Ion are 550 and 950 µA/µm, respectively, independent of the channel thickness.

Buried oxide scaling is another approach to enable L_g scaling for UTBB devices. Moreover, this drastically increases the body factor, and therefore boosts the back biasing efficiency. In 2009 and 2010 Fenouillet et al. [28,49] presented FDSOI devices with BOX thicknesses from 145 nm down to 10 nm. The final Si film thickness was around 8 nm and the nominal gate length 32 nm. It was shown that the use of a thin silicon film coupled with a thin BOX and ground plane (GP) allows improving short channel effects by reducing the lateral electrostatic coupling between the source and the drain. DIBL and subthreshold slope values were significantly reduced compared to thick BOX (Fig. 22). The simple addition of the GP to the thin BOX was a key enabler to achieve a |Vth| increase up to 130 mV for NMOS and PMOS devices (Fig. 22).

More recently, Liu et al. [50] presented FDSOI work exploring the scaling benefits of thinner BOX. In this work FDSOI devices with L_g = 20 nm were fabricated on T_{BOX} down to 15 nm. As shown in Fig. 23, both NFET and PFET DIBL were improved due to the combination of thinner BOX (20 nm compared to 25 nm) and optimized junctions. The same Figure shows also the Id/Vg curves with various back bias (Vbb) at Vdd of 0.75 V. For the NFET, the body factor (e.g. dVt/dVb) increases from 70 mV/V to 100 mV/V, with T_{BOX} thinning from 20 nm to 15 nm. For the PFET, the body factor increases from 75 mV/V to 95 mV/V. It is also worth noting that for the NFET, the GIDL floor (lowest leakage point) becomes lower when applying a negative bias, due to a lower electric field at drain side. However, the GIDL floor of the SiGe channel PFET increases when Vbb is >2 V. The change in GIDL for PFET is more pronounced with a 15 nm T_{BOX}, due to the higher electric field. As stated above, the use of a thin BOX is a solution to scale further the FDSOI technology due to the electrostatic improvement. However, another benefit of a thin BOX is that it enables more efficient back bias (V_B) capability. Indeed, the coupling between the back bias and the channel through a 10 nm thin BOX is strong. The |dVt/dVb| factor on UTBB is in between 70 and 170 mV/V, depending on the back plane doping and bias [7]. Moreover, in contrast to

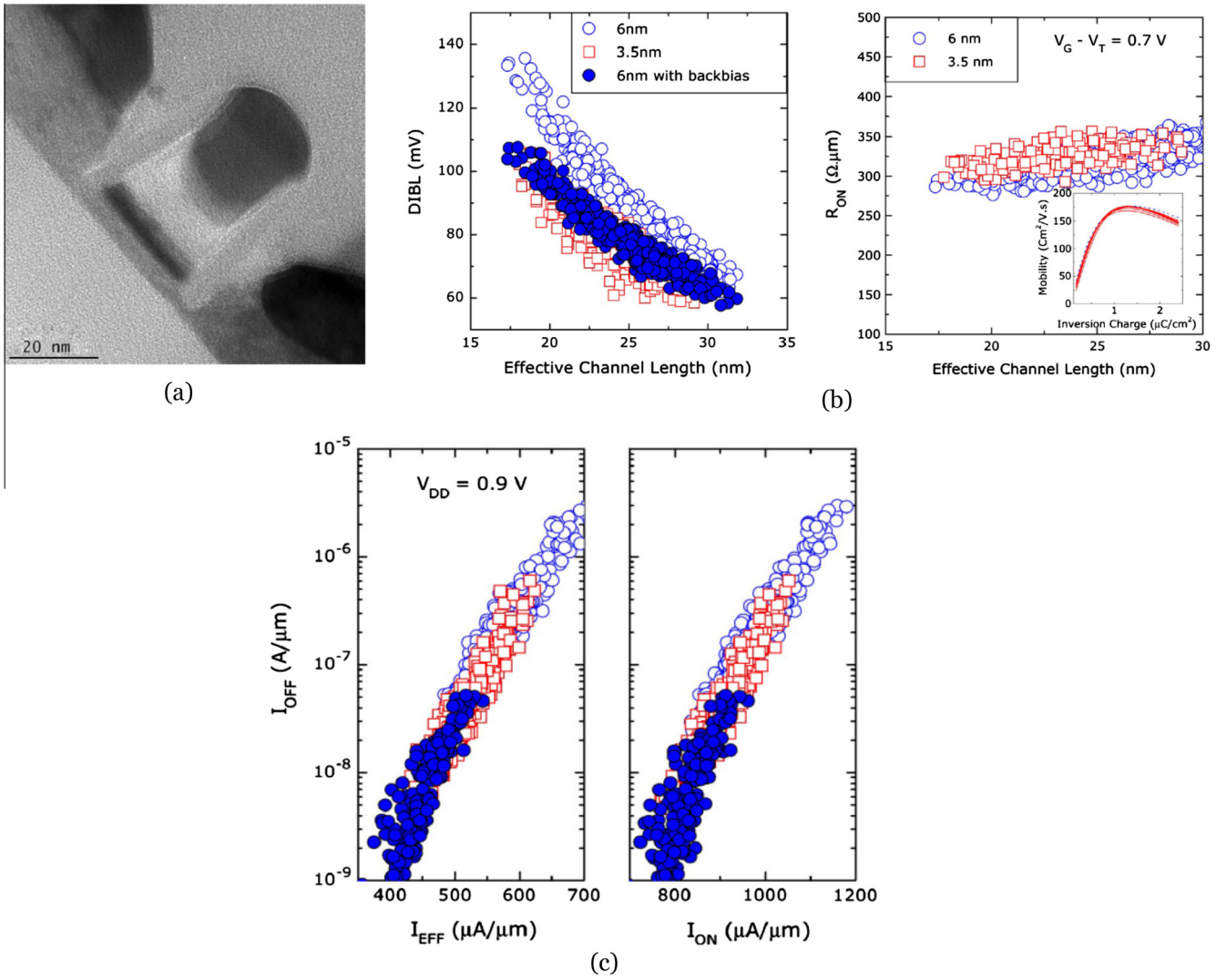

Fig. 21. After [48]. (a) High-resolution TEM cross section of ETSOI MOSFET with a channel thickness of 3.5 nm. (b) Left: DIBL characteristics of the fabricated ETSOI MOSFETs demonstrating good device electrostatics down to sub-20-nm channel length. Superior short-channel control is achieved by either thinning the channel or by applying a reverse back bias to increase carrier confinement. Linear and saturation threshold voltage are measured at *VDS* equal to 50 mV and 0.9 V, respectively. Right: Total resistance as a function of the effective channel length, showing only 20-Ω µm increase in the external resistance when channel thickness is scaled from 6 to 3.5 nm. The inset shows long-channel mobility as a function of the inversion charge, demonstrating negligible mobility degradation when the channel is thinned from (dashed line) 6 nm to (solid lines) 3.5 nm. (c) Effective and saturation current versus OFF-current characteristics of the ETSOI transistors with channel thicknesses of (open circles) 6 nm and (squares) 3.5 nm and (filled circles) 6-nm channel with reverse back bias, demonstrating no performance degradation with thinner channel or back bias.

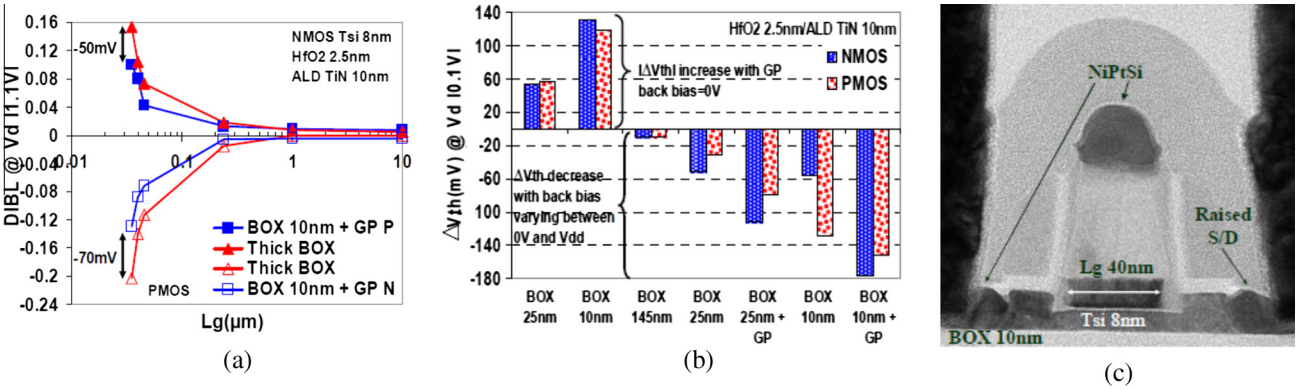

Fig. 22. After [28,49]. (a) DIBL for NMOS and PMOS devices for wafers with thin BOX 10 nm with GP and thick BOX. (b) Vth variation for devices with and without GP @ Vback = 0V (left) and Vback = Vdd for NMOS and Vback = −Vdd for PMOS devices for L_g 10 µm (right). (c) TEM picture of a FDSOI device with L_g = 40 nm and thin BOX (10 nm) with BP.

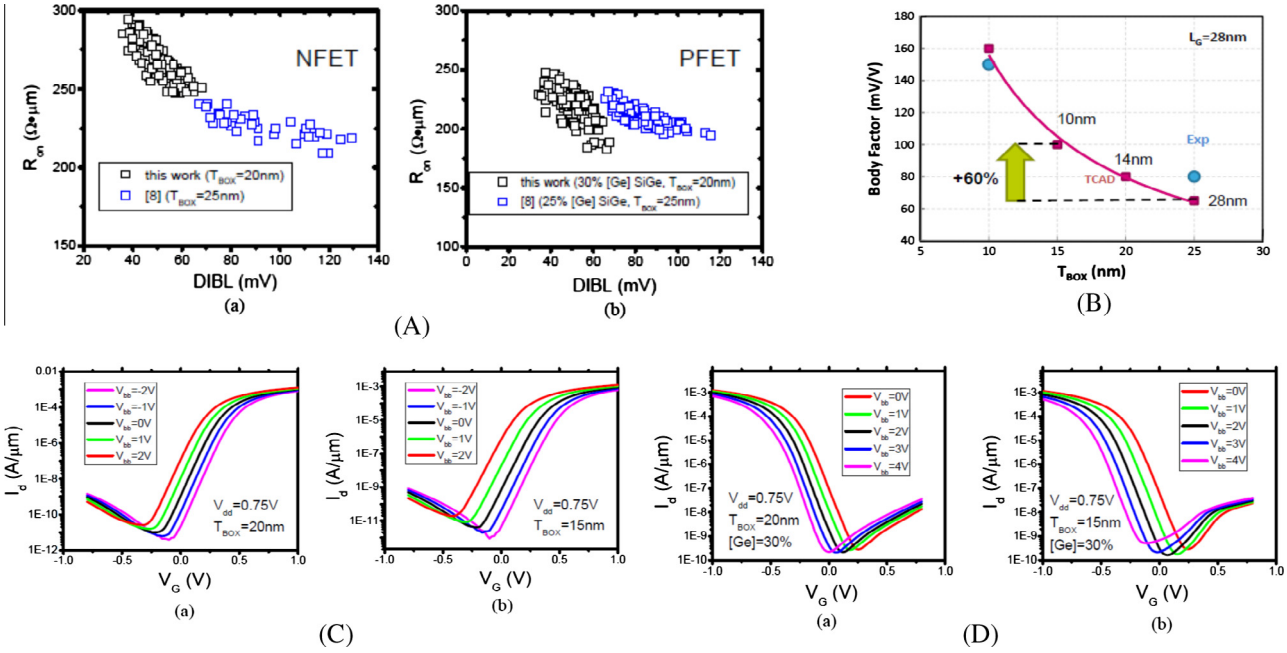

Fig. 23. After [50]. (A) The Ron/DIBL plots of (a) NFET and (b) PFET showing better DIBL with thinner TBOX and optimized junction design, comparing with data from Ref. [42]. (B) Thinning T_{BOX} from 25 nm to 15 nm improves the body factor by 60%. (C) Id/VG curves of NFET on (a)20 nm BOX and (b)15 nm BOX substrate with back bias from −2 V to 2 V, showing the larger body factor with thinner BOX. (D) Id/VG curves of PFET on (a) 20 nm BOX and (b) 15 nm BOX substrate with back bias from 0 V to 4 V. The GIDL floor starts to increase when large bias (Vbb > 2 V) is applied, which results in higher electric field and tunneling current.

bulk, the presence of the BOX in FDSOI suppresses the risk of junction leakages as long as specific processing is used to prevent junction leakage between back planes. Consequently, large back biases are possible on FDSOI, which would lead to a wide I_{ON}–I_{OFF} tuning capability. Finally, it is worth noting that the Forward Back Bias (FBB) effect is even higher at low Vdd. This can be explained by the fact that the Ion sensitivity to VB is theoretically inversely proportional to the gate voltage overdrive.

An innovative dual-depth shallow trench isolation (dual STI) scheme for Ultra Thin Body and Box (UTBB) FDSOI architecture was introduced to gain additional performance from back biasing by Grenouillet et al. [51]. In this new scheme wells were isolated from one another by the deep trenches filled with oxide as compared to junction isolation. This architecture enabled the use a much wider range of back bias voltage while staying compatible with both standard bulk design and conventional SOI substrates. As shown in Fig. 24, the dual STI architecture was designed with two Pwells (1 below NMOSFET and 1 below PMOSFET) isolated from each other by deep STI and from the P-type substrate by a deep Nwell (DNW). Within a Pwell, the flavor of the transistors can be changed by locally resorting to a shallow N-type BP (NBP) implantation. This new isolation scheme led to a considerably wider BB voltage range, only limited by the DNW voltage (generally set to the highest voltage, or tied to the highest Pwell voltage) and the Pwell/DNW junction breakdown voltage (VBD). It led to much more versatile Forward/Reverse BB (FBB/RBB) ability. This innovative back gate architecture which allows NFET and PFET to be back-biased independently was totally compatible with bulk co-integration techniques. Redesign effort was minimized leading to an easy IP portability. The substrate was biased at 0 V preserving the DNW to substrate junction in reverse.

The dual depth STI and back gate implantation design were the two key enablers for this innovative isolation scheme. Only minor complexity was added to the process flow. The challenge of the back-gate architecture – which corresponds to a shrinking of the back gate implant profiles in the depth direction compared to a conventional design – relied on the technological ability to design a Pwell which was shallower than the regular STI trench, but deep enough so that the NBP could sit on top of it. The NBP implant conditions also resulted from a trade-off: the undoped channel integrity should be preserved but at the same time a high enough doping concentration at the BOX/substrate interface was necessary to retain the BB efficiency (*i.e.* to avoid substrate depletion). The DNW limits the vertical extension of the Pwell below the deep trench to maintain a well-to-well dielectric isolation. The dual-STI architecture was demonstrated on UTBB transistors with a 25 nm BOX fabricated in a 20 nm ground rule environment. The effect of BB on the I_{on}/I_{off} plot is shown in Fig. 24. With dual STI transistors, more than 2 decades I_{OFF} reduction was possible with reverse back bias and +25% I_{ON} boost with forward back bias. Indeed, this means that frequency can be boosted by 25% with FBB at same Vdd, or a drastic decrease of the dynamic power is possible at the same frequency.

Several studies have evaluated FDSOI technology for high-performance (HP) applications. Many reports have presented the use of advanced strain-engineering techniques to boost the PMOS and NMOS carrier mobility. The literature data indicates that FDSOI can be a viable option for high performance applications.

A particular challenge for FDSOI, as well as FinFETs is mobility enhancement for NFET. Several researchers in the published literature showed that electron mobility enhancement can be achieved by using biaxially strained silicon-on-insulator (sSOI) wafers [41,46,50,52,62]. A recent and relevant report of electron mobility enhancement for aggressively scaled FDSOI NFETS is by Khakifirooz et al. in 2012 [41]. This work showed an astonishing 27% improvement in I_{eff} at a fixed I_{off} for short-channel FDSOI devices with a nominal gate length of 22 nm on sSOI channels compared to SOI control.

One significant challenge in realizing sSOI CMOS is integration of strain for PMOS. The tensile strain from the substrate enhances electron mobility by about 60% but also degrades hole mobility dramatically. Liu et al. [50] presented an integration scheme to solve the degradation of hole mobility for sSOI CMOS. In this work UTBB devices with L_g = 20 nm and 5 nm spacer featuring a tensile

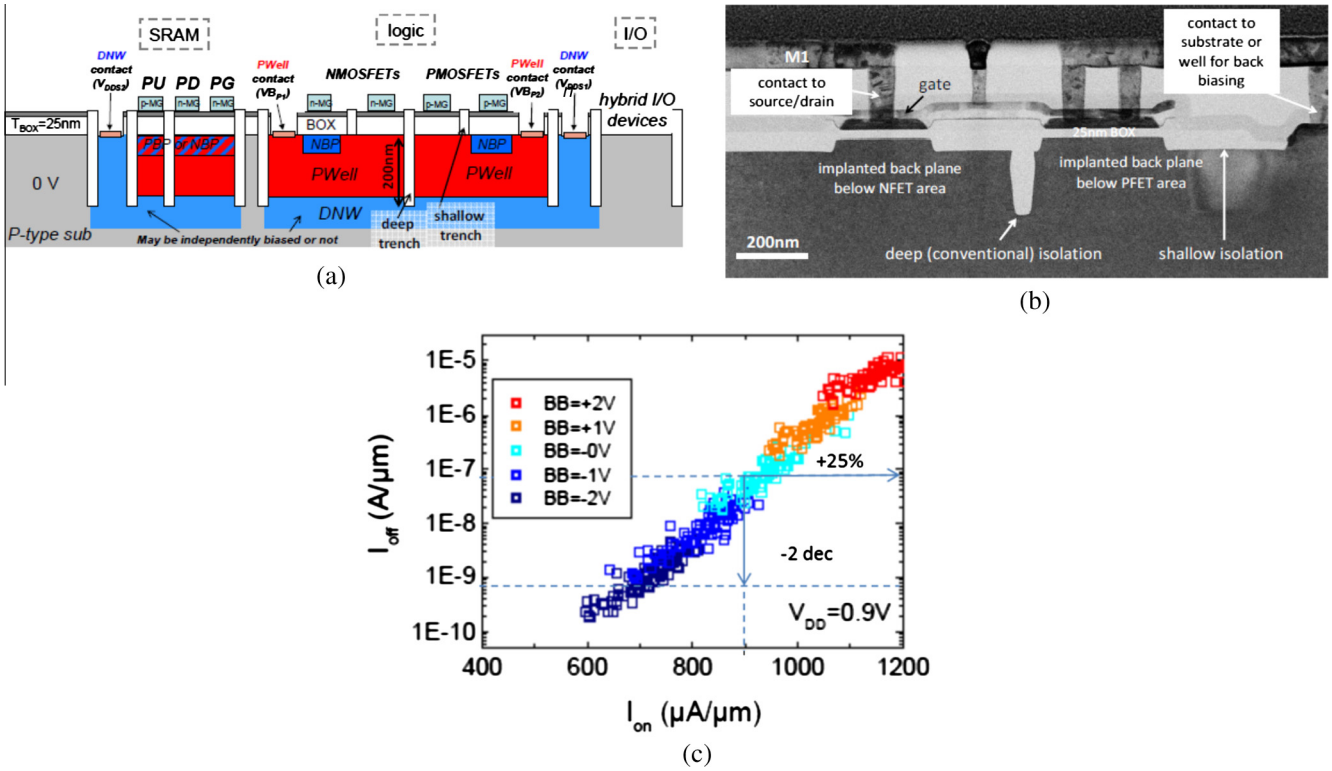

Fig. 24. After [51]. (a) Cross sectional view of a multi-Vt strategy with a planar FDSOI platform, featuring two STI depths. Deep trenches isolate NFET regions from PFET regions, whereas shallow trenches isolate individual devices. (b) STEM image featuring successful co-integration of deep and shallow trenches, and front side contact to the substrate or well for back biasing. (c) NFET I_{on}–I_{off} plot for different back bias ranging from −2 V to +2 V illustrating the gain in performance (+25%) under forward bias and the potential for energy efficiency (2 decade I_{OFF} reduction) under reverse back bias.

strained Silicon-on-Insulator (sSOI) channel NFET were demonstrated. At Vdd of 0.75 V, competitive effective current (I_{eff}) of 550/340 µA/µm was demonstrated for NFET, at I_{off} of 100/1 nA/µm, respectively. The tensile strain in the channel reduced the Vt by ~140 mV vs. a non-strained Si channel. Competitive subthreshold slope and DIBL were also reported. The electron peak mobility improved by 60% with sSOI, as shown in Fig. 25. A comparison of the reliability parameters, such as breakdown voltage (VBD) and positive bias temperature instability (PBTI), between sSOI and SOI channels, showed that the reliability of sSOI NFET was similar to that of SOI NFET, while both were superior to 20 nm Bulk NFET.

The significance of the work from Liu et al. [50] is that it demonstrated that the tensile strain in the sSOI wafer can be transformed into compressive strain. PFETs were fabricated starting with sSOI and next performing the Ge condensation technique as had been practiced for the 14 nm node PFET. The results showed measureable performance enhancement over Si devices. In addition, it was shown that for reduced channel widths there is a significant mobility enhancement, as the biaxial strain in the SiGe channel transforms into uniaxial strain along the current flow.

Recently, DeSalvo et al. presented a detailed experimental and theoretical study of the influence of Ge% and layout effects in FDSOI devices [46]. Fig. 26 shows the I_{on}–I_{off} characteristics of the cSiGe PMOS (on SOI and sSOI, with Ge up to 35%) and sSOI NMOS FD devices (featuring a 6 nm-thick channel and 20 nm gate length). The performance advantage of strained SiGe channel for PMOS devices over relaxed Si clearly appears (with a gain

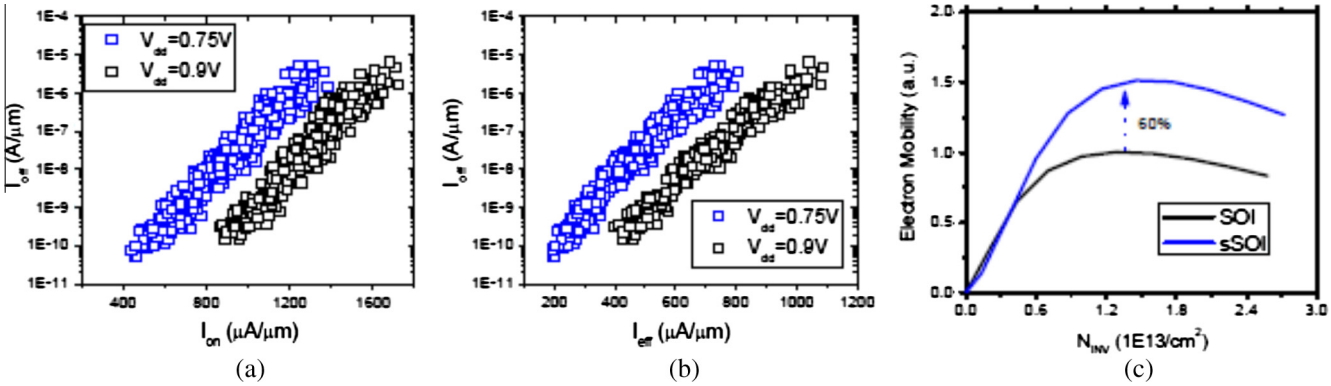

Fig. 25. After [50]. sSOI NFET (a) Ion and (b) I_{eff} at Vdd of 0.9 V and 0.75 V. At Vdd = 0.75 V, and I_{off} of 100 nA/µm and 1 nA/µm, the Ion reaches 1120 µA/µm and 760 µA/µm, while I_{eff} reaches 610 µA/µm and 360 µA/µm, respectively. (c) NFET mobility plot showing that a 60% improvement of electron peak mobility is obtained at the same SOI thickness.

increasing with the Ge content, up to 65% for 35%Ge). Note also that the same Figure demonstrates the strain reversal of sSOI by SiGe in short channel devices (35%Ge on sSOI yields to a 16% current gain). Fig. 26 also shows that narrow cSiGe PMOS devices with uniaxial strain, the transverse strain (detrimental for hole mobility) being fully relaxed, show the best performance. An Ion gain of 90% is achieved shrinking the device width to 80 nm.

The low field mobility (μ0) in short channel devices was extracted using the Y-function methodology (which allows for series resistance effect suppression). To explore layout effects, the mobility was studied versus the gate length (L_g), width (W) and active area length (Lact). Fig. 26 shows a 60% mobility gain measured on long, large sSOI transistors compared to SOI, due to tensile biaxial stress. A significant mobility enhancement was also achieved while increasing the Ge content in cSiGe PMOS, thanks to compressive biaxial strain. In both unstrained/strained devices, the mobility decreases for short gate lengths due to defect-enhanced scattering rates close to S and D region (as neutral and/or Coulombian centers) or to ballistic effect.

The short channel mobility gain extracted in Fig. 26 was higher than the one obtained in long channel devices, due to stronger effects of RSD stressors with short gate length. In NMOS, even low activated SiCP RSD grown on sSOI are tensile and generate more stress than in unstrained SOI. No variation of μ0 is observed versus Lact and W in unstrained PMOS/NMOS. A strong layout effect appears in cSiGe PMOS, where the narrowing of the active width to 80 nm leads to +60% μ0 enhancement (in full agreement with the Ion measurements). On the other side, when Lact

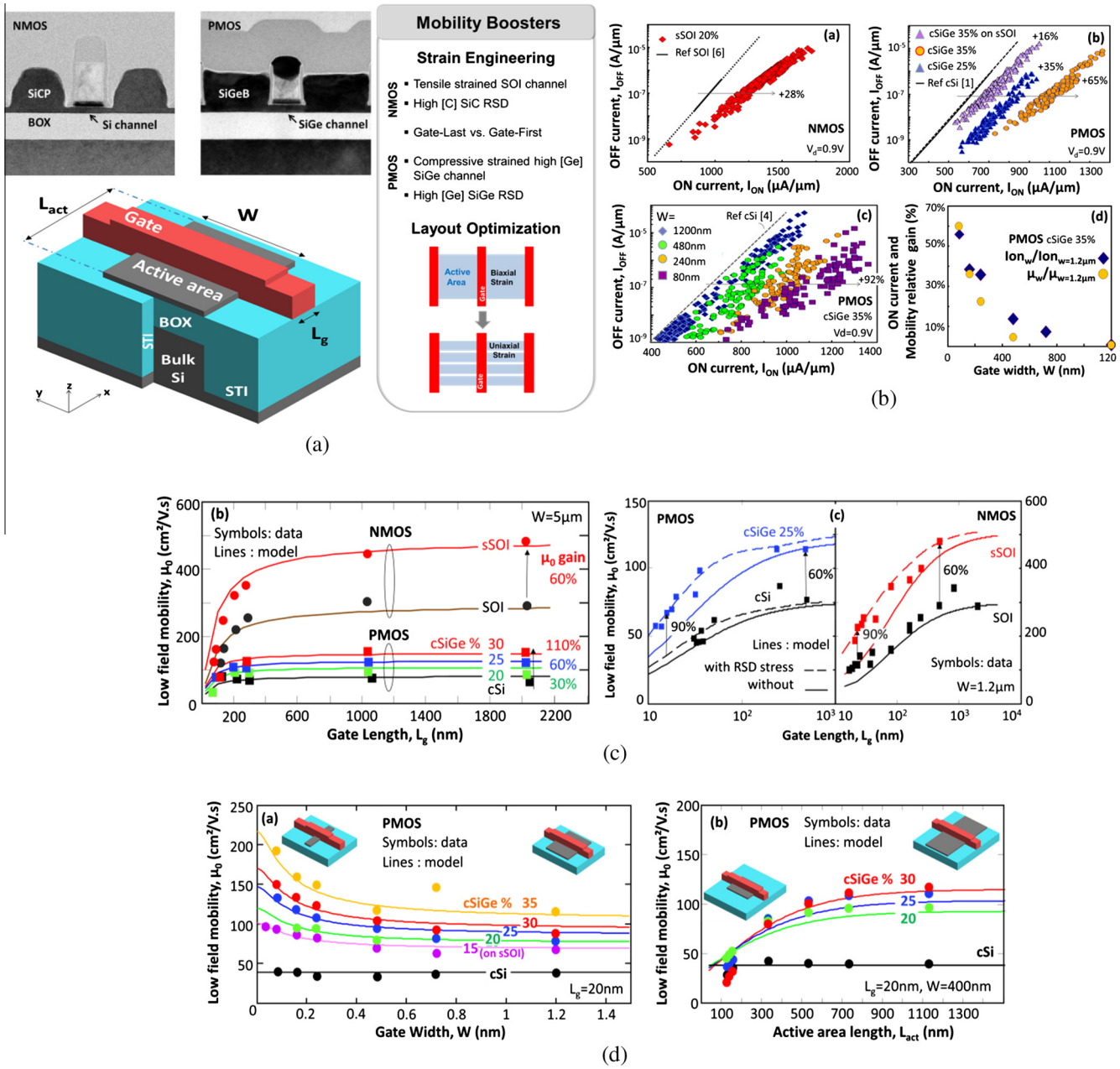

Fig. 26. After [46]. (a) TEM images and schema of the NMOS/PMOS FDSOI devices. The mobility boosters explored in this paper are indicated on the right. (b) I_{on}/I_{off} of (a) SOI/sSOI NMOS, (b) cSi/cSiGe PMOS on SOI (sSOI), (c) 35% cSiGe PMOS with different W. (d) 35% cSiGe PMOS I_{on} (μ_0) gain versus W. (c) PMOS/NMOS mobility versus gate length L_g, (lin-lin plot (b) or lin-log plot (c)). (d) cSi/cSiGe PMOS mobility versus gate width, W (a) and active area length, L_{act} (b).

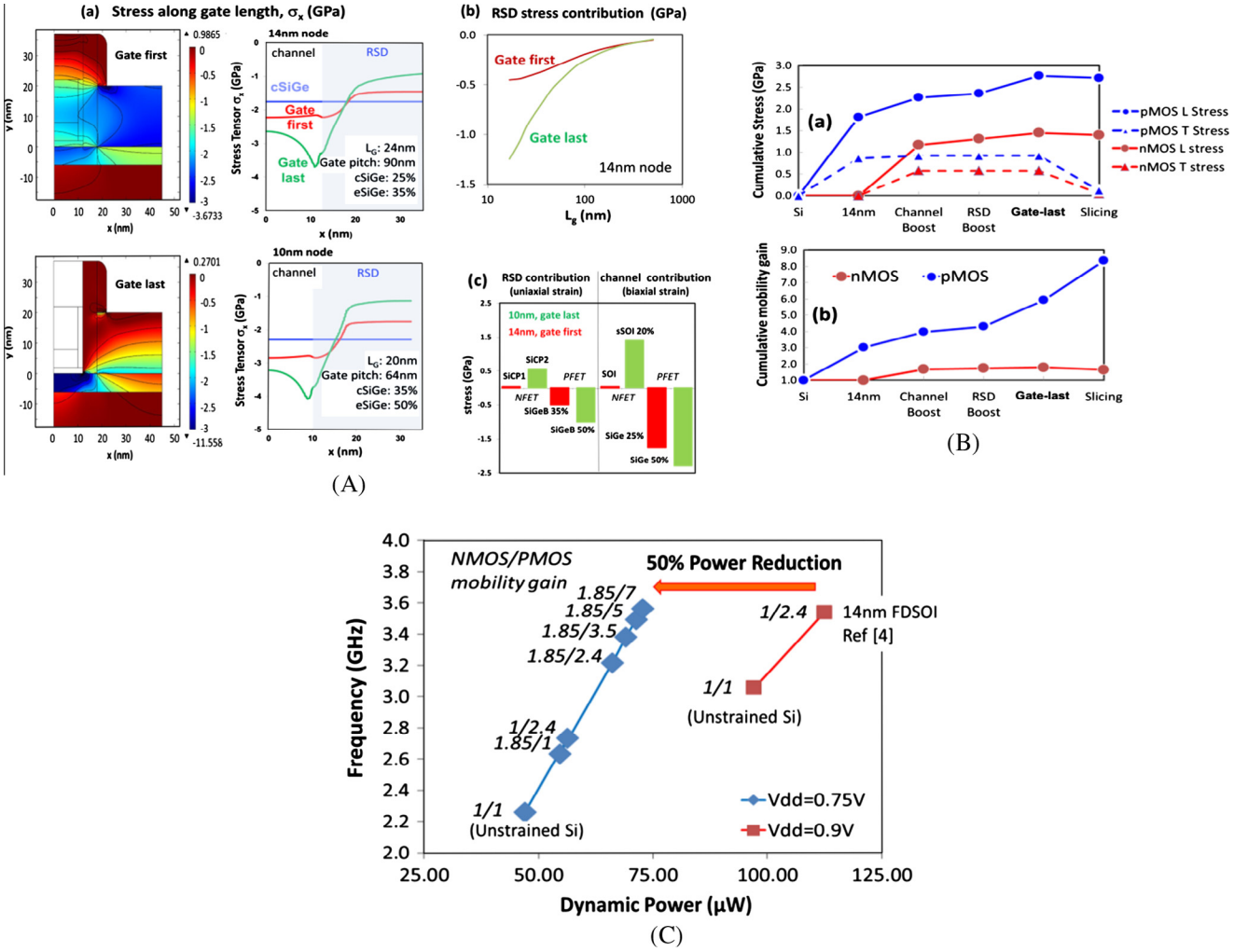

Fig. 27. After [46]. (A) 2D FEM mechanical simulations: (a) contribution of cSiGe channel, channel and Raised Source Drain, with gate-first/last, to PMOS stress. (b) RSD stress contribution vs transistor gate length. (c) Summary of NMOS/PMOS stress contributions in nominal 10/14 nm standard cells, considering the decreased pitch and transverse/longitudinal strain values based on 3D simulations. (B) Variation of transverse and longitudinal strain for NMOS/PMOS stressors (from 3D mechanical simulations of 14/10 nm nominal cells). (b) Corresponding mobility gain, by the analytical model. *Note that carrier transport along the* (001) *Si planes presents a significant bonus for electrons* versus *holes, thus more hole mobility gain allows for n/p mobility balance.* (C) Oscillator circuit simulations (assuming same device geometries for PMOS and NMOS, FO = 3 and 1.5fF parasitic capacitances) showing the reduction in dynamic power by reducing the V_{dd} from 0.9 V to 0.75 V, while maintaining frequency performance through PMOS/NMOS mobility boosters.

decreases, a mobility gain degradation happens. A completely different behavior is obtained for sSOI NMOS, showing a weaker layout dependence.

In [46] a multi-level modeling of stress engineering design in next-generation power-efficient FDSOI devices was presented. Starting from 3D mechanical simulations and piezoresistive coefficient data, an original, simple, physical-based model for holes/electrons mobility enhancement in strained devices was developed. The model was calibrated based on physical measurements and electrical data of state-of-the-art devices. Non-Equilibrium Greens Function (NEGF) quantum simulations of holes/electrons stress-enhanced mobility gave physical insights into mobility behavior at large stress (~3 GPa). Finally, the new strained-enhanced mobility model was introduced in an industrial compact model to project performance at the circuit level. To evaluate the effectiveness of embedded RSD stressors in scaled devices with decreased gate pitch, we calculated the channel stress induced both with cSiGe channel and eSiGe RSD as function of Ge fraction, and study the impact of a replacement gate process compared to a gate first process (Fig. 27). It appeared that the strained channel provides the largest stress contribution, while moderate stress comes from RSD and gate last.

An analytical model for stress-enhanced mobility was developed [46]. For holes, the mobility gain was assumed exponentially dependent on the longitudinal/transverse stress (instead of being linearized). For electrons, an empirical law is used inspired by piezoresistive coefficients and quantum simulations. The stress channel and SD profiles from 3D mechanical simulations were included in the mobility computation. Figs. 26 and 27 show that the model captures very well the stress effects, independently of device type and Ge%. Fig. 27 shows the variation of longitudinal and transverse stresses with the key stressors modules (both for n and p type devices). The longitudinal stress magnitude was increased, whereas the transverse stress was reduced. The corresponding mobility gain induced by each stressor, computed by means of mechanical simulations and mobility analytical model as presented above, was also shown. sSOI substrate provides the major NMOS gain (x2), whereas PMOS mobility is improved by a factor 8 both by Ge fractions increase in channel/RSD and by layout optimization (slicing) to reduce the transverse stress component.

The new stress-enhanced mobility model was included in the UTSOI2 SPICE model [53]. Pre-layout ring oscillators were simulated either with unstrained or strained P/NMOS devices at different V_{dd} (Fig. 27) showing that a dynamic power gain of 50% could be achieved while maintaining circuit frequency performance by introducing efficient mobility boosters. So, by means of a multi-scale model, calibrated with measurements, a clear scaling path to achieve high mobility, power-efficient sub-14 nm FDSOI technologies was identified.

Finally, it should be mentioned that other modules are currently under investigation to further enhance FDSOI performance. Among them, it is worth to mention: Self Aligned In Plane Stressors (SAIPS) for mobility improvement [54]; T_{inv} scaling to improve electrostatics and increase I_{eff} [50]; Replacement Metal Gate (RMG) for mobility enhancement [55,46]; sSOI relaxation in PFET region before condensation, for hole mobility improvement in sSOI CMOS [56,57] or alternative sSOI fabrication approach to improve NMOS mobility [58–60].

3. Conclusions

In this paper, we provided a historical review of the main research and development efforts done in the last decade to realize planar FDSOI devices in the 28 nm technology node and beyond, in the frame of the joint development program between IBM, CEA-LETI and ST Microelectronics. FDSOI advantages include excellent electrostatics, excellent mismatch performance due to the undoped channel, effective back bias for Vt control/performance boost and power management. Technology demonstration has been proven at 28 nm and 14 nm nodes and feasibility has been shown for 10 nm node and beyond. High performance devices at low supply voltage are achievable at aggressive ground rules due to the implementation and effectiveness of strain engineering techniques in planar UTBB FDSOI. Moreover, FDSOI brings an easy manufacturing path to develop high performance and low power CMOS. This simple planar technology and transistor architecture offers tremendous flexibility to the SoC design via the body biasing strategies for dynamic power optimization. Recently, major foundries have committed to the production of FDSOI at 28 nm and 22 nm, thus supporting the development of an FDSOI ecosystem.

All these elements make FDSOI technology one of the strongest contenders for continued CMOS technology scaling. FDSOI technology is particularly well suited for low cost, low voltage, and energy efficient applications.

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