Ultra-thin body & buried oxide SOI substrate development and qualification for Fully Depleted SOI device with back bias capability

Walter Schwarzenbach *, Bich-Yen Nguyen, Frederic Allibert, Christophe Girard, Christophe Maleville

Soitec | Parc Technologique des Fontaines, 38190 Bernin, France

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ABSTRACT

This paper reviews the properties of the SOI wafers fabricated using the Smart Cut™ technology, with ultra-thin body and buried oxide (BOX) required for the FD-SOI CMOS platform. It focuses on the parameters that require specific attention for this technology, namely, the top silicon layer thickness uniformity and buried oxide reliability. The first one is linked to the threshold voltage variability and the second to the active role played by the BOX when a back-bias is used. An overview of the specific process optimization and metrology developed to achieve the targeted specifications is given.

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1. Introduction

Portable, digital electronics and wireless communication markets have increased tremendously in the last five years, driving worldwide semiconductor sales in 2015 to over \$350B according to the Semiconductor Industry Association [1]. Electronic consumers demand for more functionality, smaller form factor or lighter weight, longer battery life and lower cost. This means transistor scaling should follow Gordon Moore's law and Robert Dennard's scaling rule without compromising performance, power, area or cost. However, as gate lengths approach sub-45 nm dimensions and gate oxides approach 1 nm, scaling becomes more challenging, and new material and device structures are required to overcome the fundamental physical limitations imposed by traditional semiconductor materials. The obstacles to continuing the reduction of transistor dimensions can be traced to threshold voltage and gate oxide thickness that cannot be scaled at the same rate as supply voltage (V_{dd}) without leakage current exceeding stand-by power requirements for portable electronics applications. Thus, transistor scaling rapidly reduces the maximum gate overdrive factor, Cox (V_{dd}–V_T) [2] or transistor drive current (I_d), which is a measure of device/circuit performance. Moreover, higher channel doping concentrations and more abrupt, shallow source-drain junctions used to control short-channel effects at very short gate lengths result in carrier mobility degradation, increasing threshold voltage variability, junction leakage, and capacitance. In response, many in the industry have switched to Fully-Depleted transistors for better short channel effect and smaller variability. Two flavors have been proposed: planar Fully-Depleted Silicon-On-Insulator (FD-SOI) [3] and FinFET on Bulk Silicon [4] or on SOI starting wafers [5].

2. Planar Fully Depleted devices for extending CMOS scaling

FD-SOI with ultra-thin BOX (Buried OXide), known as Ultra-Thin-Body and BOX (UTBB) substrate, is an attractive candidate for extending Moore's Law at 28 nm and beyond while keeping the cost benefit from shrinking. FD-SOI devices represent an extension of the planar device architecture demonstrating several key advantages needed for low power and ultra-low power circuits. FD-SOI devices have excellent immunity to soft-error-rate and short channel effects leading to improved sub-threshold swing and drain-induced barrier lowering, thus it improves performance and/or power. FD-SOI devices also use the undoped channel resulting in much lower threshold voltage variation due to minimizing random dopant fluctuation [6,7]. This enables operation-voltage scaling for reducing active power consumption and improves SRAM and analog mismatch and gain, allowing superior digital/analog co-integration and area saving [8]. Other unique feature of FD-SOI on thin BOX substrate is the back-bias capability [9], which enables threshold voltage (V_T) tuning for better performance/power trade-off without degradation (Fig. 1) and more cost effective solution than fabricating different V_T transistors using channel doping or work-function tuning [7]. The flexibility allowed by the back-bias, and the intrinsic value of the technology for energy efficient computing have been illustrated through several applications, including an FPGA (Field-Programmable Gate Array) demonstrating successful operation down to voltages at and below the minimum energy point of the circuit [10]. Compared to the standard 1.2 V operating voltage of the FPGA, a 13× reduction in
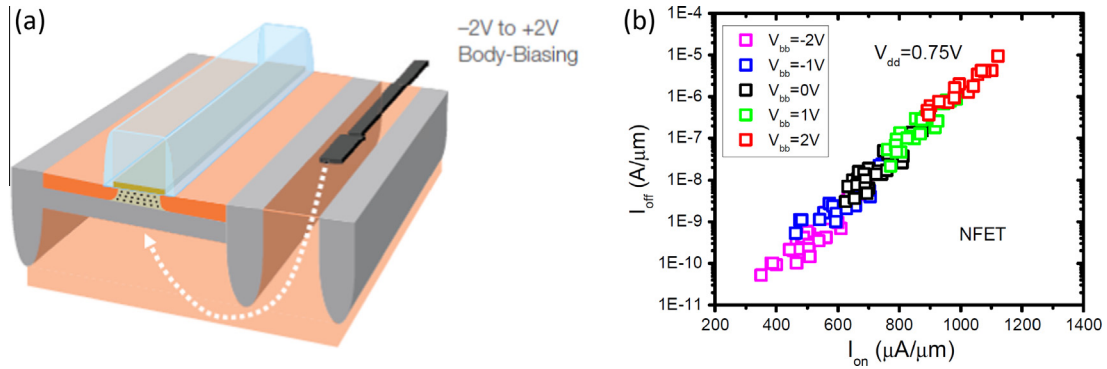
* Corresponding author.

Fig. 1. (a) FD-SOI with back bias [11], (b) ion vs. Ioff with back-bias up to ±2 V [12].

Power-Delay-Product was achieved through a combination of low voltage operation and fine-grained back-biasing, enabled by the very thin BOX.

Another illustration came from a direct comparison between 28 nm LPDC (Low-Density Parity-Check) decoders fabricated simultaneously in bulk and FD-SOI technologies [11]. Flatresse et al. demonstrated, on 28 nm FDSOI, 49% power reduction or 35% speed gain versus 28 nm bulk for performance oriented designs and 10X leakage reduction versus bulk for low standby power applications.

The planar FD-SOI devices are fully compatible with mainstream CMOS processing, designs and EDA tools. This allows retaining a low-disruption planar approach for low process/design cost and fast time to market, but it puts tight requirements on starting wafers, which demands extremely thin and uniform silicon and buried oxide layers. Wafer manufacturers have worked to fulfill these needs and are now able to reach atomic-level control of thin silicon and oxide thicknesses. These wafers are in production ramp and ready for high volume manufacturing. This paper reviews the Smart Cut^{TM} process optimization, quality of the thin SOI and BOX substrate, and substrate roadmap for scaling down to 10 nm node.

3. Smart Cut^{TM} process for FD-SOI substrate

The Smart Cut^{TM} process, Fig. 2, is based on wafer bonding and hydrogen implantation to transfer an ultra-thin silicon on oxide layer from a defect free high quality donor substrate to a handle wafer. This uses the same Smart Cut process-steps as other SOI products (partially depleted SOI devices), which have been in high volume manufacturing for well over a decade. Thus FD-SOI substrate development benefited from 20 years of layer-transfer learning and volume production expertise. However, extensive optimization of the Smart Cut^{TM} process is still essential for delivering ultra-thin SOI and BOX films with well controlled wafer-to-wafer and within-wafer uniformity [13]. To retain the excellent V_T variation and for tightening performance/leakage distribution, an SOI film uniformity within ±5A (3-sigma) is required and has been demonstrated [14,15]. To meet these requirements, the process focuses on (1) a highly uniform thermal oxidation of a donor wafer to form the thin BOX with good electrical properties; (2) a conformal hydrogen implant through the oxide to define the separation plane in the silicon, (3) a high temperature anneal to eliminate the local SOI roughness while keeping excellent on-wafer SOI uniformity. Further tightening of the wafer-to-wafer average thickness distribution is then obtained through Adaptive Process Control (APC), which consist in tuning the finishing steps according to the average wafer thickness after the high temperature anneal [16].

3.1. SOI product roadmap

SOI product roadmap for Planar Fully Depleted devices, reported on Fig. 3, includes several product generations. UTBOX, or UTBB substrates are designed for initial technology nodes starting at 28 nm, including thin unstrained SOI and BOX layers on high quality silicon substrates with adapted orientation. These materials are now in High Volume Manufacturing production or in risk production mode in Soitec lines. Soitec's product roadmap already anticipates advanced material needs, including the use of high mobility materials with strained Si and SiGe ([Ge] up to 80%, including tensile or compressive strains) top layers. These engineered substrates serve as basis for advanced device integration schemes targeting boosted performance [17,18].

3.2. SOI thickness metrology

To ensure low transistor V_T variability, SOI thickness monitoring across the full spatial frequency range is required. This range of spatial frequencies corresponds to dimensions (or wavelengths) from ~10 nm to 30 cm (wafer size) to fully cover the within-wafer thickness uniformity. It is also necessary to cover the average wafer-to-wafer thickness variations. Fig. 4 illustrates such spatial frequency domains with corresponding metrology & and typical variations [15].

At wafer level, ellipsometry gives access to SOI & BOX thicknesses. Using a properly defined 41 pts (points) map, as described on Fig. 5a, allows a correct evaluation of the within-wafer thickness range. This is confirmed by comparing measurements results obtained with said 41 pts map (Fig. 5b) to a more detailed mapping (725 pts, Fig. 5c). Both maps yield the same measurement accuracy, exhibiting ±0.5 nm wafer scale thickness variations. The 41 pts map obviously gives a higher measurement throughput (tens of wafers per hour, >15 times faster w.r.t. 725 pts), to be compatible with industrial requirements.

Since the ellipsometer is capable of covering wavelengths ranging from sub-millimeter to tens of centimeters, it enables uniformity inspection covering spatial wavelength corresponding to "die-to-die" and "wafer-to-wafer" scales.

At sub-micrometer level (typically below 5 μm wavelength), well known atomic force microscopy metrology can be used to monitor device-scale thickness variations. Fig. 6 shows excellent, <1 A RMS on 30 × 30 μm² scan, results obtained on FD-SOI substrates [19]. However, AFM only gives access to the surface variations, not to the SOI film thickness variations. Though surface roughness is relevant to transistor properties, Si uniformity is the main parameter of interest.

To address the SOI uniformity in a wavelength range from 1 μm to 100 μm, a dedicated measurement technique called differential
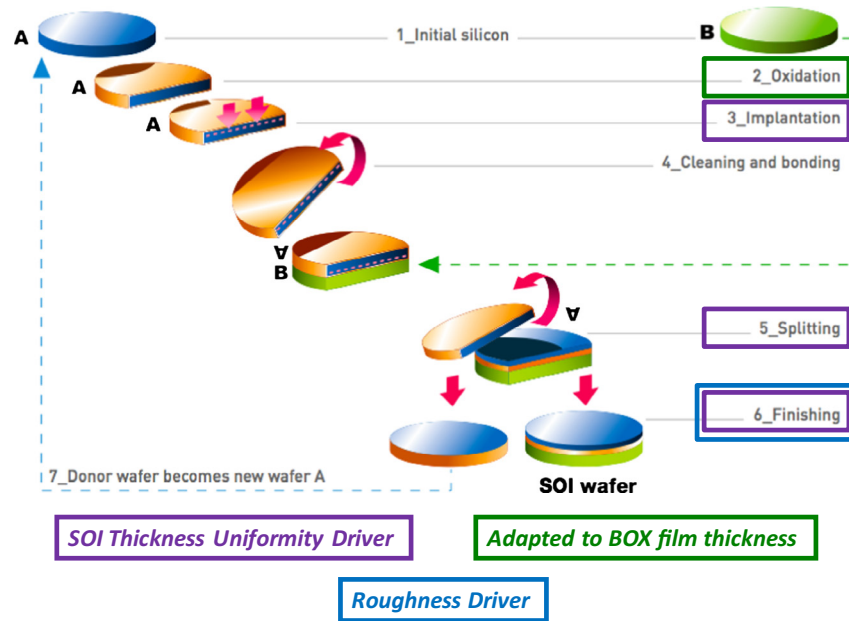
Fig. 2. Smart Cut™ process adapted for FD-SOI material.

Fig. 3. Soitec product roadmap for FD-SOI substrates.

reflective microscopy (DRM) was developed. It enables measuring the thickness in a range of wavelengths covering the within-die and cell-to-cell variability. The technique is based on the variation of the intensity of the reflected light when the SOI layer thickness varies. To maximize the measurement's precision, the wavelength is selected such that sensitivity to BOX thickness variations is minimized. Associated with an optical microscope, digital camera, and proper image-treatment algorithms, it leads to average, sigma & peak to valley SOI thickness output over a typical $80 \times 60\ \mu m^2$ field of view [20,21]. This methods, schematically described on Fig. 7, is now routinely available for production monitoring, on various FD-SOI thickness stacks.

3.2.1. SOI thickness control at wafer scale – wafer-to-wafer

Applications based on PDSOI wafers have high thickness-uniformity requirements, typically ±1 nm wafer-to-wafer [16]. This was achieved thanks to process and line optimization and tool-to-tool matching.

With FD-SOI, thickness uniformity requirements become extremely stringent and wafer to wafer variations are reduced down to ±0.1 nm. Fig. 8 describes the tailored cleaning, specifically implemented. This APC module implemented in the FD-SOI line does not induce any significant cost & cycle time impact and can be adapted on either batch or single wafer cleaners. Processes are fully automated.

Fig. 9 shows typical mean SOI thickness distribution on 10,000 production wafers, with and without such specific treatment, demonstrating a wafer to wafer variation improved down to ±0.1 nm.

3.2.2. SOI thickness control at wafer scale – within-wafer uniformity

FD-SOI tight within-wafer uniformity is obtained through an optimization of the process steps, previously described on Fig. 2, combining [22].

– Near-perfect condition for oxide growth, which leads to (i) BOX layer uniformity (Fig. 10a) and (ii) reduction of the implantation depth (i.e. fracture plane) variations.
– Optimized implant & splitting anneals for post splitting performance (Fig. 10b).
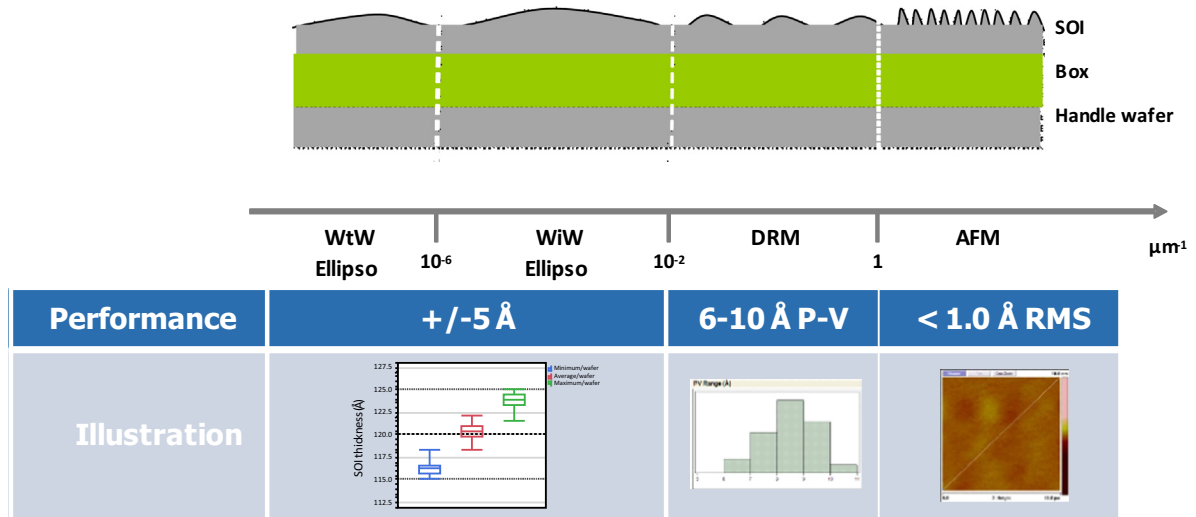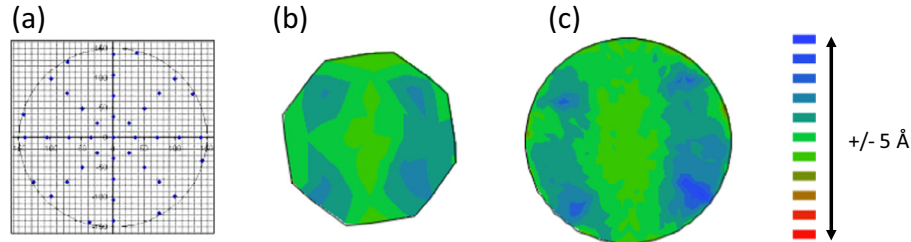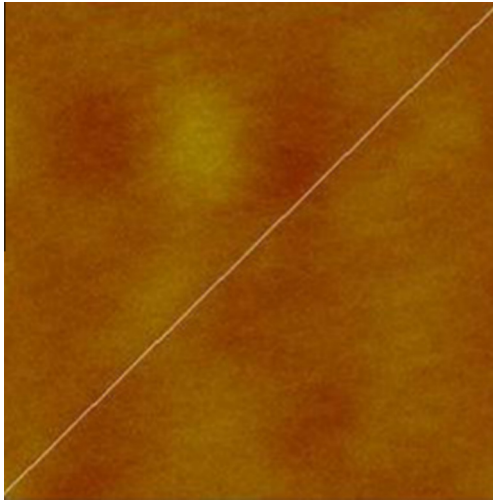
Fig. 4. SOI layer thickness control.

Fig. 5. (a) 41 pts ellipsometry mapping (b) 41 pts mapping (c) 725 pts extended SOI thickness map of production 120/250 A SOI/BOX wafer. Both mapping show thickness variation range within 1 nm.

Fig. 6. AFM scan, 30 × 30 μm², on FD-SOI substrate.

– Adapted finishing steps (sacrificial oxidation steps, smoothing anneal process) (Fig. 10c).

Fig. 10 shows typical on-wafer film and BOX thickness uniformity evolution across the SmartCut process flow, for a single substrate in the median of the production distribution.

Combining wafer to wafer & within wafer thickness variations, Fig. 11 illustrates a ±0.5 nm SOI thickness control, all points, all wafers, over an FD-SOI manufacturing volume of thousands of wafers. To keep things in perspective, this means less than 5 silicon inter-atomic distances over a 300 mm wafer.

3.2.3. SOI thickness control at device scale – roughness & high frequency variability

Device scale thickness variation is monitored through micro-roughness performance, including AFM & DRM metrologies. In addition to conventional Smart Cut process step optimizations, several finishing options have been evaluated, aiming to reduce the final SOI surface roughness while keeping excellent on-wafer SOI uniformity and industrial capability [23].

The use of Chemical-Mechanical-Polishing processes allow excellent roughness performance but currently induces significant on-wafer SOI uniformity degradation, even with limited Si removal. As shown on Fig. 12, the on-wafer uniformity is steadily degraded after incremental thickness removals.

Thermal smoothing through the surface diffusion process, as described by Mullins–Herring surface diffusion equation [24], allows reducing surface roughness with a limited impact on wafer-scale SOI uniformity. Fig. 13 shows AFM results on several UTBOX substrate options. In contrast to the $\geqslant 0.3$ nm RMS on $30 \times 30 \ \mu m^2$ fields Partially Depleted SOI products, UTBOX for Fully Depleted applications exhibits a 0.08 nm $30 \times 30 \ \mu m^2$ RMS. Corresponding peak-to-valley performance, as measured with DRM metrology, is improved from 2 nm (PDSOI) down to 0.8 nm (FD-SOI substrates).

Thus, Fig. 14 illustrates, through a Power Spectral Density (PSD) vs. Spatial frequency curve from a $30 \times 30 \ \mu m^2$ AFM scan, that Smart Cut finishing process optimization allows FD-SOI substrate to reach a surface smoothness similar to polished bulk.
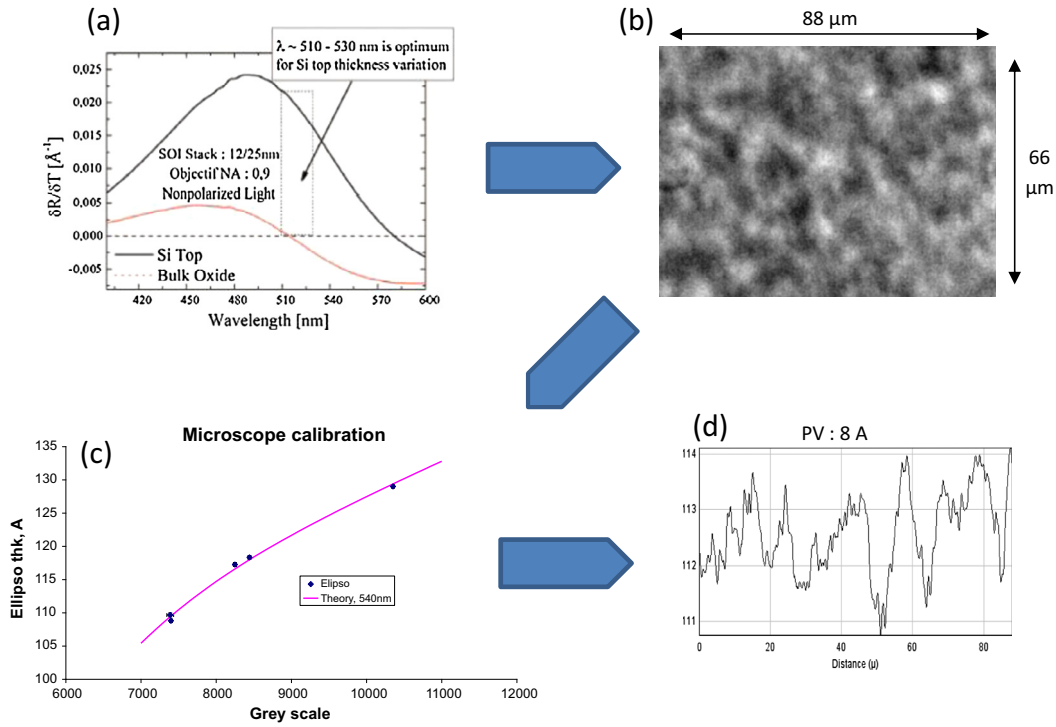
Fig. 7. DRM schematics, (a) SOI & BOX reflectivity vs wavelength for 120/250 A stack, (b) typical gray scale optical microscope field of view, (c) digitalized gray scale vs thickness correlation, (d) 120/250 thickness variation scan [20].
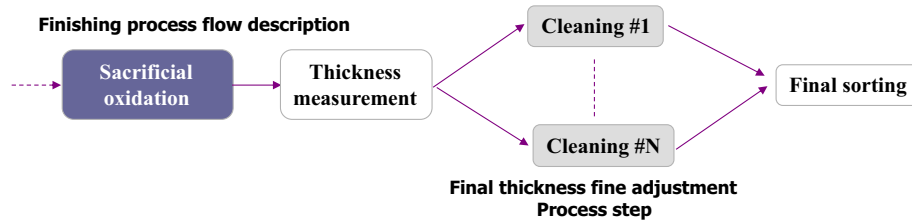

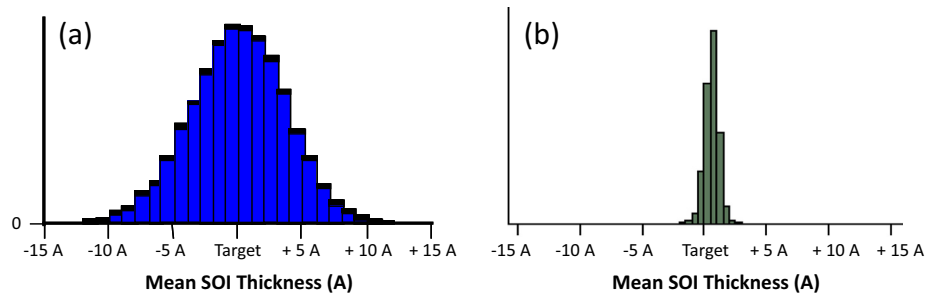**Fig. 8.** Specific FD-SOI cleaning tailoring schematics for wafer to wafer thickness control.

Fig. 9. Wafer to wafer SOI mean thickness distribution, (a) PDSOI generation, (b) FD-SOI generation.

3.3. UTBOX defect density performance

SOI surface defectivity is measured with a threshold as low as 50 nm using KLA Tencor SP3® tools [25]. SOI defectivity is reduced through the optimization of all Smart Cut conventional process steps: oxidation, implant – splitting, bonding & finishing. It allows UTBOX materials to reach best bulk quality levels. Fig. 15 compares defectivity distribution measured on an SP3 at 50 nm threshold on polished silicon bulk and on final 12/25 nm UTBOX substrate. As advised by the ITRS roadmap, measurement threshold should be

further reduced. Initial measurements on SP5 show promising results, for even lower threshold inspection down to 29 nm.

3.4. BOX layer – extended scale & electrical reliability

FD-SOI substrates for 28FD & 22FD technology nodes are designed with a BOX layer of 25 or 20 nm. BOX layer thickness is controlled within ±1 nm. BOX thickness reduction down to 10 nm has been developed using the Smart Cut process, in order to enable the FD scaling path thanks to improved electrostatic
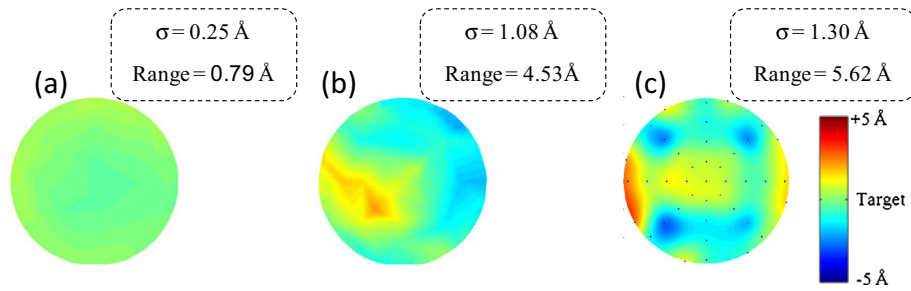
Fig. 10. Ellipsometry 41 pts within-wafer uniformity over process steps, showing a thickness range of (a) 0.08 nm after BOX formation, (b) 0.45 nm after splitting and (c) 0.56 nm on finished SOI [22].
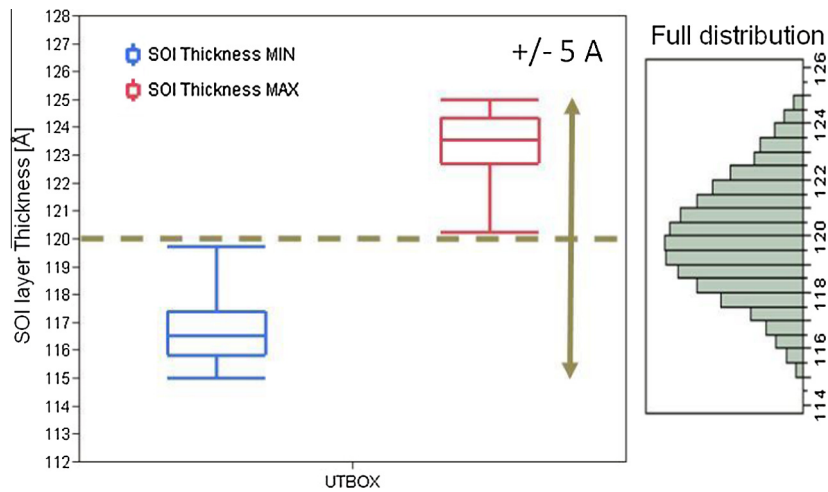

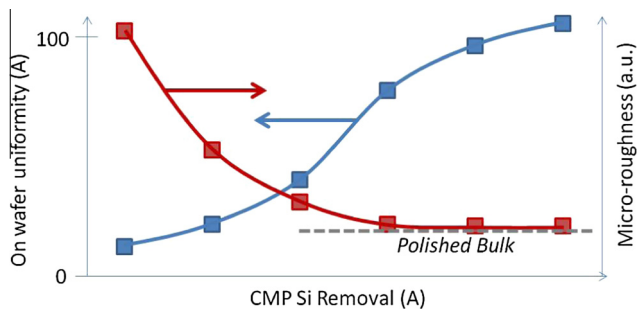**Fig. 11.** Production FD-SOI wafers: thickness distribution [22].

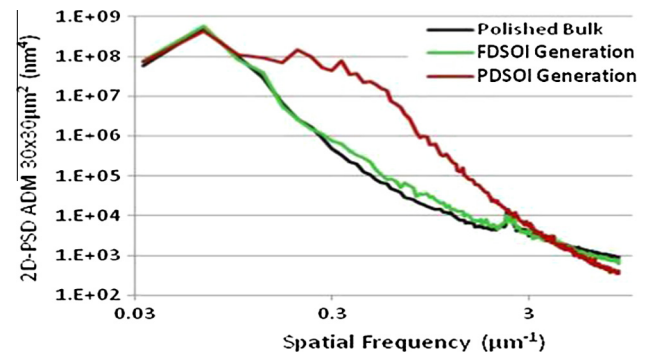**Fig. 12.** On wafer uniformity & micro-roughness measured through SP2 Haze vs. CMP Si removal [23].

Fig. 14. Power spectral density (PSD) from $30 \times 30\ \mu m^2$ AFM scans for polished bulk, PDSOI & FD-SOI substrates [23].
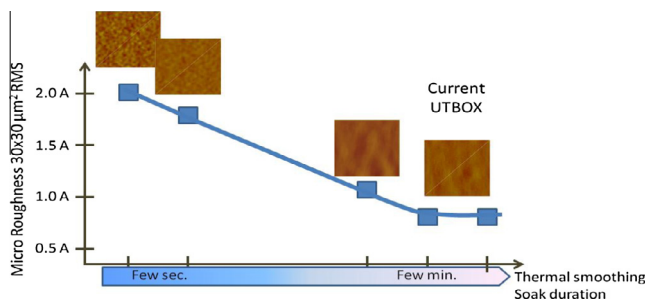

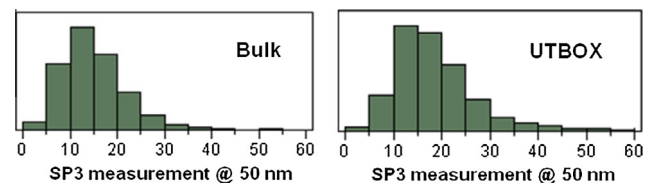**Fig. 13.** AFM micro-roughness performance vs finishing thermal smoothing [23].

Fig. 15. Measured SP3 defectivity distribution @ 50 nm threshold on (left) Si bulk & (right) final UTBOX [23].
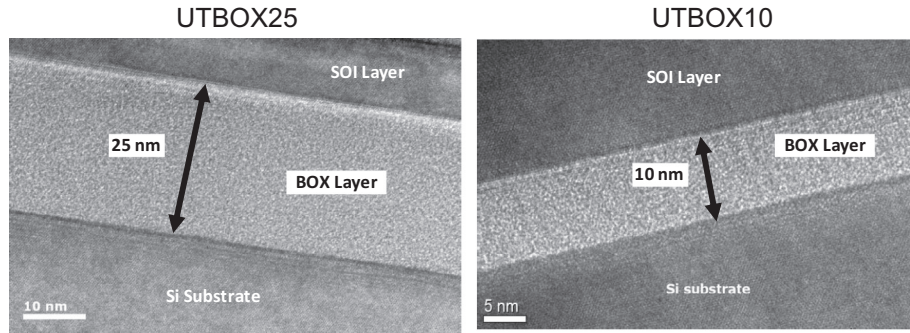
UTBOX25   UTBOX10

Fig. 16. BOX TEM cross section for (left) UTBOX25 & right (UTBOX10) [24].
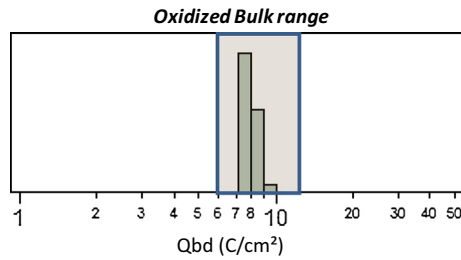

Fig. 17. UTBOX charge to breakdown, BOX 25 nm, with reference to oxidized bulk (light gray band).
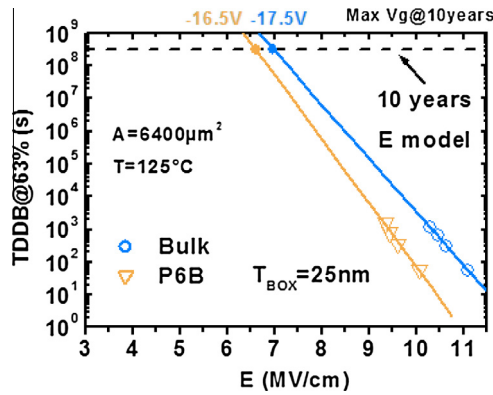

Fig. 18. TDDB, oxidized bulk & FD-SOI substrate [27].

control via the back gate [26]. Fig. 16 shows typical TEM cross sections of BOX 25 nm & 10 nm thicknesses, associated with ultra-thin SOI.

Buried oxide layer benefits for PDSOI substrate include device to device and device to substrate electrical isolation, leading to possible isolation of 3D structures. For FD-SOI applications, BOX layer electrical reliability checklist needs to take into account the active role associated with back-bias modulation. In addition to good resistance to breakdown, low leakage, low electrical pinhole density requirements from previous substrate generations, [27] BOX layer needs to demonstrate good ageing behavior through charge to breakdown (Qbd) & time dependant electrical breakdown (TDDB) measurements.

Charge to breakdown (Qbd) values up to 10 C/cm^2 are measured on finished 25 nm BOX FD-SOI substrates [27]. Fig. 17 reports such distribution, as measured on finished FD-SOI materials from volume production, similar to 6–10 C/cm^2 25 nm oxidized bulk reference.

Fig. 18 reports the high-field BOX TDDB measurements along with the low-field extrapolation, assuming a linear relationship between breakdown and electric field [28]. On a 25 nm BOX, an operating voltage of 16.5 V is derived to reach the 10 years lifetime requirements, which is well above the actual back-bias voltages (±3 V) and similar to values obtained on an oxidized and annealed silicon reference, confirming reliability retention after the Smart Cut process.

Fig. 19 reports consistent & stable D_{IT} & Q_{BOX} values, from C(V) measurements, on both Partially & Fully Depleted SOI technologies, whatever BOX thickness, in the absence of forming gas anneal. These expected low values, observed at the end of the SOI fabrication process, are related to relatively high thermal treatments occurrence.
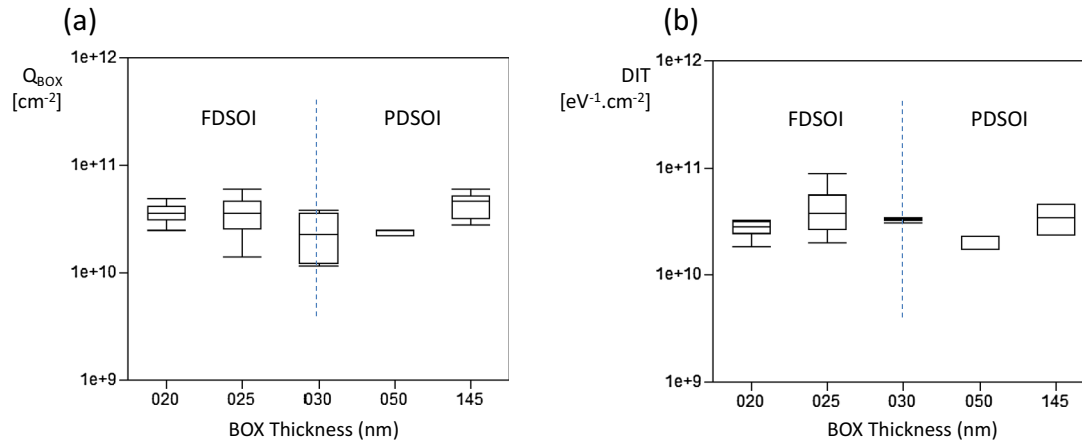

Fig. 19. (a) QBOX & (b) DIT measured vs BOX thickness [27].

4. Conclusion

Engineered SOI substrates with excellent quality, roughness and uniformity are now a mainstream option for the semiconductor industry adopted by several foundries. UTBB FD-SOI substrates enable planar Fully Depleted devices with full back bias capability to extend Moore's Law at 28 nm and beyond providing excellent power/performance/area/cost benefits, especially at very low operation voltage. Combining advanced CMOS process capabilities with the demonstrated benefits of engineered SOI substrates is paving the way for digital and analog/RF integration for next generation cost-sensitive integrated ULP mobile connected devices. Thus, engineered SOI substrates are well positioned to serve future mobile communication and integrated IoT/wearable applications.

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