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A review of electrical characterization techniques for ultrathin FDSOI materials and devices

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ABSTRACT

The characterization of nanosize SOI materials and devices is challenging because multiple oxides, interfaces and channels coexist. Conventional measurement methods need to be replaced, or at least updated. We review the routine techniques that proved efficient for the evaluation of bare SOI wafers (essentially the pseudo-MOSFET) and of MOS structures (transistors and gated diodes). Informative examples are selected to illustrate the typical properties of advanced SOI wafers and MOSFETs. We will show how the ultrathin film and short-channel effects affect the interpretation of the experimental data.

1. Introduction

The future landscape of the micro-nano-electronics industry is subject of debates, strategic decisions and ... question marks. Whether the ultimate device will be FinFET [1], nanowire [2,3], planar SOI [4,5] or 3D [6] is not clear yet. The winner is expected to cumulate fast transport capability, electrostatic integrity and reliability. The old couple Si-SiO_2 is gradually giving way to more talented materials such as high-k dielectrics and strained Ge or III–V semiconductors.

Two trends are however ineluctable: the CMOS scaling will continue and, from now on to the end of the avenue, the MOS transistor will operate in fully depleted (FD) mode. Electrostatic considerations impose the body of the transistor to be sub-10 nm thick (hence FD) in at least one direction, vertical or lateral, and preferably controlled by multiple gates. An oxide underneath the body is a clear asset for dielectric isolation and back-biasing schemes.

For these reasons, we believe that the planar Semiconductor-On-Insulator technology (SOI) is the simpler solution to date. State-of-the-art SOI MOSFETs combine ultrathin strained body, thin buried oxide (BOX), short high-K/metal gates, and take advantage of substrate biasing. In these FD devices, the evaluation of basic parameters, such as carrier mobility and lifetime, threshold voltage, or oxide and interface defects, is no longer straightforward. Multi-channel coupling and thickness/length nanosize effects modify not only the measured value, but also the meaning of classical parameters. The optimization of SOI materials, device integration modules, compact models and design libraries requires increasingly accurate characterization able to address sub-10 nm thick structures.

This paper is not aimed as an exhaustive encyclopedia of the numerous techniques and variants elaborated mainly for thick SOI materials and devices. Instead, we focus on practical methods that, according to our experience, proved to be efficient and relatively easy to implement in ultrathin films. The following section describes the generic methods for measurement and parameter extraction using as test vehicles MOS transistors and diodes. In Section 3, we discuss in detail the material evaluation and typical properties. The pseudo-MOSFET is an indisputable technique which has recently been enriched with advanced modules. It can be complemented with back-gated Hall effect and Second Harmonic Generation measurements. Section 4 is dedicated to FDSOI transistors and shows the variation of the key device parameters (threshold voltage, mobility, subthreshold slope and leakage current) with film thickness, back-bias and strain. We finally discuss the impact of short-channel effects and other scaling-related mechanisms (coupling and supercoupling, parasitic bipolar transistor, floating body). Guidelines for measurement strategies and accurate interpretation of the experimental data are suggested.

2. Characterization techniques and associated parameter extraction

The techniques selected and discussed in this section can be applied indifferently to front and/or back-gate measurements.

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For simplicity, we will refer to 'front' and 'back' channels although these notions are less and less appropriate as the SOI film becomes thinner. In ultrathin FDSOI, the carriers induced by one gate tend actually to spread in the entire film; 'volume' inversion/accumulation [7,8], rather than a charge-sheet surface channel, is often prevalent.

2.1. Current-based methods in MOSFETs

In advanced MOSFETs, the drain current in linear regime (low drain voltage) versus the applied voltages and the geometry of the transistor can be written as [9]:

$$I_D = \frac{W}{L} \cdot \frac{\mu_0}{1 + \theta_1 \cdot (V_G - V_T) + \theta_2 \cdot (V_G - V_T)^2} \cdot C_{OX} \cdot (V_G - V_T) \cdot V_D \quad (1)$$

where W and L are the width and the length of the transistor, μ_0 is the low-field mobility, V_G and V_D are the applied voltages on the gate and on the drain, V_T is the threshold voltage, and θ_1 and θ_2 are the mobility attenuation factors due to series resistance and surface roughness, respectively.

I_D–V_G curves are measured, for a given V_D, with the aim of extracting the parameters V_T and μ_0, based on Eq. (1). The non-linear dependence of I_D versus V_G requires specific treatment. We will describe the usual methods (Y-function, double derivative and McLarty) as well as their application conditions in the next sections.

2.1.1. Y-function method

This method is widely used for the transistors in which the θ_2 term is negligible, i.e. the vertical electric field in the channel is sufficiently low, such as the surface roughness does not play an important role in the mobility reduction. In this configuration, I_D in Eq. (1), and the associated transconductance, g_m, can be written as:

$$I_D = \frac{W}{L} \cdot \frac{\mu_0}{1 + \theta_1 \cdot (V_G - V_T)} \cdot C_{OX} \cdot (V_G - V_T) \cdot V_D \quad (2)$$

$$g_m = \frac{dI_D}{dV_G} = \frac{W}{L} \cdot \frac{\mu_0}{[1 + \theta_1 \cdot (V_G - V_T)]^2} \cdot C_{OX} \cdot V_D \quad (3)$$

The direct use of these two equations is not practical due to the non-linearity induced by θ_1 factor. The Y-function, defined to eliminate θ_1 [10], is straightforward to apply:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \cdot \mu_0 \cdot C_{OX} \cdot V_D} \cdot (V_G - V_T) \quad (4)$$

After the channel formation ($V_G > V_T$), Y has a linear dependence versus V_G (see Fig. 2a for MOSFET and Fig. 17 for pseudo-MOS). Its intercept with the V_G-axis yields the threshold voltage, while the slope gives the low-field mobility. Coefficient θ_1 is determined from the slope of $1/\sqrt{g_m}(V_G)$ line. Since $\theta_1 \approx R_{SD} \cdot \mu_0 \cdot C_{OX} \cdot W/L$, the series resistance R_{SD} can be evaluated.

Note that this simple method is effective for fully fabricated MOSFETs, as well as for pseudo-MOSFET. The limitations are related to the hypothesis of negligible impact of surface roughness on the mobility. Practically, after tracing the Y-function versus the gate voltage, the linearity of the curve indicates the appropriateness of this method.

2.1.2. Double derivative

The second derivative method was developed to eliminate the dependence on the series resistances that induces inaccuracy in the threshold voltage extraction. Additionally, this extraction technique is not affected by the mobility degradation [11,12]. The threshold voltage is the gate voltage corresponding to the peak of the transconductance derivative, *i.e.*, the second derivative of the drain current (Fig. 1). In FDSOI devices, the peak of the second derivative of front-channel $I_D(V_{G1})$ characteristics yields the front threshold voltage for different conditions at the back interface. When the front and the back channels are activated (Fig. 1b), the second derivative curve exhibits two peaks [13–15].

The main drawback of this method comes from the high sensitivity to measurement errors and noise. Indeed, the use of the second derivative data treatment leads numerically to a high-pass filter [11]. The $I_D(V_G)$ measurements should be performed with very small steps ($\Delta V_G < 10$ mV). The threshold voltage detected by the second derivative corresponds qualitatively to the one provided by the first derivative of the gate capacitance-voltage characteristics (see also Section 2.3.3).

2.1.3. McLarty method

In order to account for surface roughness effects, which increase rapidly with vertical field, the simple formulation of the effective mobility in Eq. (2) needs to be enriched as in Eq. (1):

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 (V_G - V_T) + \theta_2 (V_G - V_T)^2} \quad (5)$$

The second mobility attenuation factor θ_2 can lead to a negative transconductance at high V_G; its physical meaning is explained in [16]. Whether θ_2 is important or not can be deduced by drawing the Y-function. If $Y(V_G)$ plot is linear, θ_2 can be safely ignored. When θ_2 is relevant, it leads to an upturn of the $Y(V_G)$ plot, as shown in Fig. 2a and expressed by:

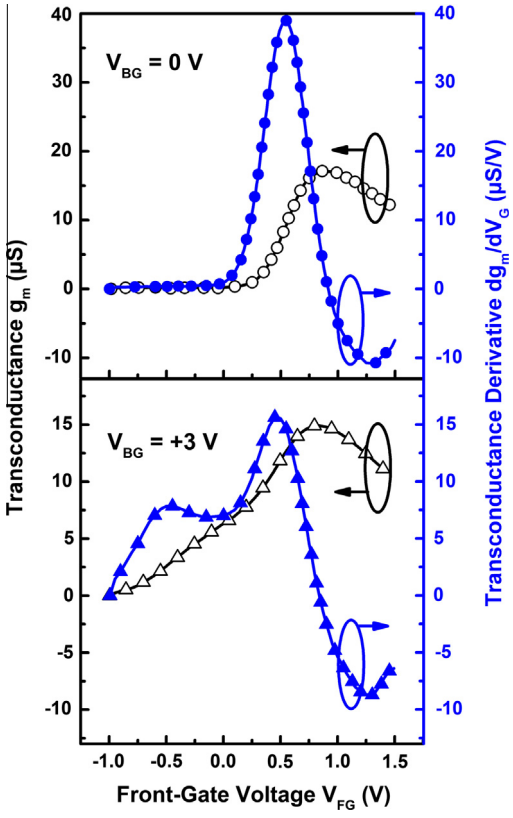

Fig. 1. Transconductance and transconductance derivative versus front-gate voltage. (a) $V_{BG} = 0$ V: the peak indicates the threshold voltage. (b) $V_{BG} = +3$ V: the two peaks show the consecutive activation of the back channel (for $V_{FG} = -0.5$ V) and front channel (for $V_{FG} = +0.5$ V).

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L}\cdot\mu_0\cdot C_{OX}\cdot V_D}\cdot(V_G - V_T)\cdot\frac{1}{\sqrt{1-\theta_2\cdot(V_G-V_T)^2}} \quad (6)$$

In this case the *Y*-function cannot be used and needs to be replaced by the McLarty's technique [17]. The principle of the development is the same, namely use the derivatives of the transistor resistance (V_D/I_D) to eliminate successively coefficients θ_1 and θ_2:

$$\frac{\partial}{\partial V_G}\left(\frac{1}{I_D}\right) = \frac{1}{A}\left(\theta_2 - \frac{1}{(V_G-V_T)^2}\right) \quad (7)$$

and

$$\frac{\partial^2}{\partial V_G^2}\left(\frac{1}{I_D}\right) = \frac{1}{A}\frac{2}{(V_G-V_T)^3} \quad (8)$$

where $A = C_{OX}\cdot\mu_0\cdot V_D\cdot W/L$.

The threshold voltage and mobility can be obtained by plotting the following function versus V_G, as illustrated in Fig. 2b:

$$\left(\frac{\partial^2}{\partial V_G^2}\left(\frac{1}{I_D}\right)\right)^{-1/3} = \left(\frac{2}{A}\right)^{-1/3}(V_G - V_T) \quad (9)$$

The threshold voltage is given by the intercept with *X*-axis and the mobility by the slope of the linear line. Coefficients θ_2 and θ_1 are determined by replacing the values of A and V_T in Eq. (7) and in drain current equation, respectively. The effective channel length is evaluated by measuring transistors with different lengths and plotting $1/A$ as a function of the designed gate length.

This extraction technique is efficient essentially if the measurements are performed with small increments in V_G such as to reduce the noise generated by the calculation of the second derivative.

2.2. Split capacitance in MOSFETs

Under the 'capacitance-based' label, one can find various methods, applied to MOS capacitors, transistors and gated diodes. For example [18]:

- *C–V* measurements on MOS capacitors for extraction of the Equivalent Oxide Thickness (EOT) of the gate dielectric, interface trap density (D_{it}), fixed oxide charge density (Q_{OX}), doping level, etc.
- Split-*CV* on MOSFETs to determine the effective mobility.
- Conductance versus frequency in split-*CV* on MOSFETs to evaluate D_{it}.
- Quasi-static *CV* to obtain D_{it}.

In this section, we will focus on split-*CV* measurements which are more amenable in FDSOI.

The current-based methods (*Y*-function, etc.) yield the threshold voltage, the low-field mobility and the mobility attenuation factors, from which the effective mobility can be reconstructed with Eq. (5). The merit of split-*CV* measurements on MOSFETs is to provide directly the effective mobility as a function of the inversion charge. The split-*CV* method is based on the separation of the contributions of substrate and channel capacitances [19,20]:

- C_{bulk}, measured between the gate and the substrate, with source and drain grounded; this option is irrelevant in FDSOI.
- C_{gc}, measured between the gate and the channel (interconnected source and drain), with the substrate grounded ($V_{BG} = 0$ in Fig. 3). The mobility extraction proceeds from combined C_{gc} and drain current curves.

During the split-*CV* measurement, a constant voltage modulated with a small-amplitude signal of fixed frequency is applied to the gate and the associated impedance is measured. A simple circuit model (typically parallel) is used to identify the capacitive term and the conductance term. The analysis of the conductance term versus the measurement frequency can give access to the interface state density. Meanwhile, the capacitive term at a fixed frequency (low enough, to avoid any parasitic resistance effects) yields the mobility.

The method calculates the inversion charge density versus gate voltage, by integrating the capacitance, from a V_G value in accumulation (where no inversion charge is present and the measured capacitance equals 0, unless parasitic capacitance effects are important) to the desired value of V_G:

$$Q_{inv}(V_G) = \int_{V_{G\_accumulation}}^{V_G} C_{gc}(u)\cdot du \quad (10)$$

The $I_D(V_G)$ characteristic is measured in parallel, and then the effective mobility is given by:

$$\mu_{eff}(V_G) = \frac{L}{W}\cdot\frac{I_D}{Q_{inv}(V_G)\cdot V_D} \quad (11)$$

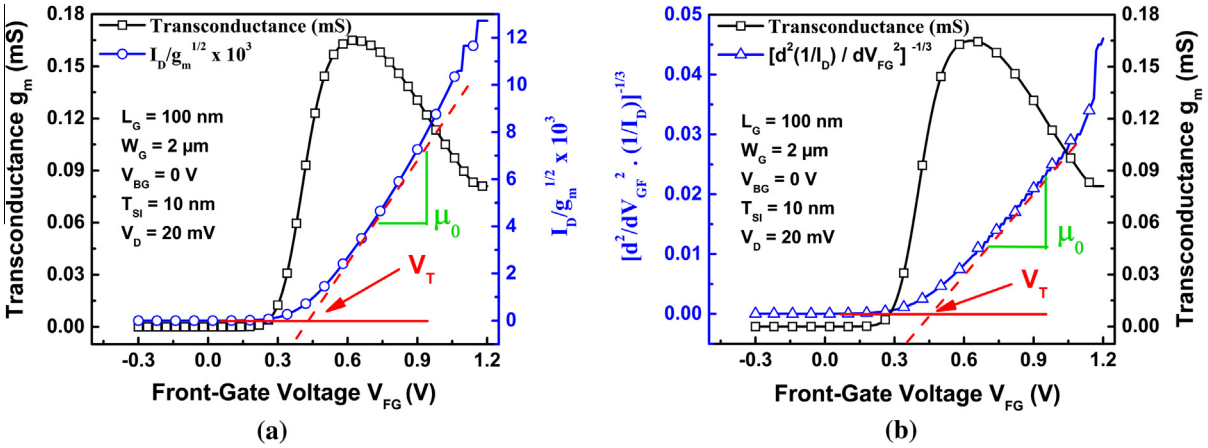

Fig. 2. (a) Typical non-linearity of *Y*-function induced by the contribution of the second mobility attenuation factor θ_2. (b) Quasi-linear curve from Eq. (9) and transconductance as a function of front-gate bias showing threshold voltage and carrier mobility extraction by McLarty method. FDSOI MOSFET with 10 nm thick body (courtesy of S.J. Chang).

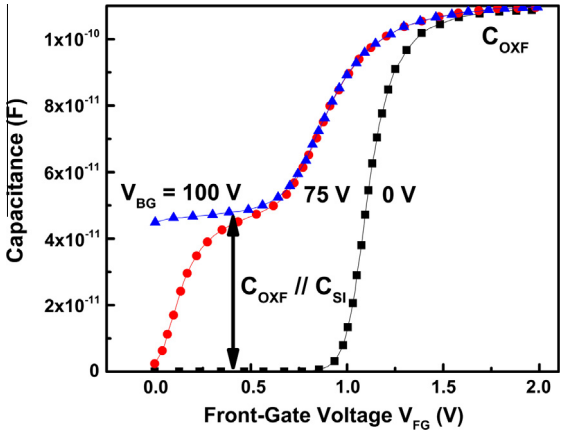

Fig. 3. Split *C–V* capacitance versus front-gate voltage for 3 typical conditions of the back channel: depleted (V_{BG} = 0), inverted (V_{BG} = +100 V) and in intermediate state. FDSOI n-channel MOSFET with 16 nm thick film, 400 nm thick BOX, and long channel (adapted from Ohata et al. [21]).

The measurement precautions include the choice of amplitude and frequency of the small signal. The V_G–scan direction can also be important, especially if charging effects of the oxide/interface traps are investigated.

The split-*CV* method usually serves to determine the front-channel mobility. In FDSOI MOSFETs, the biasing of the back gate opens additional opportunities, as shown in Fig. 3 [21]. For high bias (V_{BG} = +100 V), the back channel is inverted and the capacitance plateau reflects the series combination of oxide capacitance and depleted film capacitance, from which the film thickness is extracted.

Even more interesting is the case of intermediate bias (V_{BG} = +75 V in Fig. 3): increasing V_{FG} first opens the back channel, so the capacitance increases from zero to the plateau level. Integrating the capacitance in this region yields the back-channel charge. In other words, the back-channel mobility is evaluated from front-gate measurements. In the right-hand region of the curve (V_{FG} > 0.7 V), the capacitance increases again indicating the formation of the front channel and giving the corresponding effective mobility [21].

2.3. Measurements with gated diodes

The benefit of gated p–i–n diodes for FDSOI characterization is two-fold:

- Since diodes are co-integrated with MOSFETs, they deliver additional information about the very same CMOS process.
- The N^+ and P^+ terminals offer prompt supply of electrons and holes, enabling the body to be at equilibrium. Unlike the MOSFET, the diode is not prone to transient effects induced by the slow generation of majority carriers (see Section 2.4.3). In many respects, a diode behaves as a body-contacted 5-terminal MOSFET without being affected by the large series resistance of the body contact in ultrathin SOI technology. For this reason, the body contact is actually no longer a standard option in FDSOI design.

There are several types of measurements on gated diodes including current (Sections 2.3.1 and 2.3.2), capacitance (Section 2.3.3) and charge pumping (Section 2.3.4).

2.3.1. Reverse current

In a reversed-biased p–i–n diode (Fig. 4a), the current is governed by the carrier generation in the body and at interfaces. The relative impact of these two mechanisms can be adjusted by changing the gate bias. The typical variation of the reverse current with gate voltage $I_R(V_G)$ is reproduced in Fig. 4b and reveals several regions of operation.

For negative bias ($V_G < V_{FB}$), holes are accumulated at the interface and within the body, so the modest current I_1 originates from the junctions leakage. As soon as V_G exceeds the flatband voltage V_{FB}, the interface becomes depleted and massively contributes to the leakage current which sharply increases to I_2 value. Then the depletion region grows with V_G leading to more active bulk generation. The small increase in current from I_2 to I_3 yields the bulk generation lifetime τ_g [22,23]:

$$I_3 - I_2 = q \cdot \frac{n_i}{2} \cdot \frac{W_{D,\max}}{\tau_g} \cdot L \cdot W \tag{12}$$

where L and W are the length and width of the body and $W_{D,\max}$ is the maximum extension of the depletion region.

When the threshold voltage is reached, the inversion layer of electrons inhibits the surface generation process which results in a current drop from I_3 to I_4. The interface generation velocity S_g is obtained from the excess current [22]:

$$I_3 - I_4 = \left(q \cdot \frac{n_i}{2} \cdot S_g\right) \cdot L \cdot W \tag{13}$$

As S_g is proportional to the interface trap density, the leakage current and charge pumping current can be correlated for the detailed evaluation of the capture cross-section [24].

The left- and right-hand edges of the curve in Fig. 4b indicate the flatband and threshold voltages. Increasing the reverse bias makes the threshold voltage to increase and the plateau level to expand to the right.

The model above explains correctly the behavior of thick partially-depleted SOI diodes but has to be revisited for the case of FDSOI. When the body volume is much reduced, most of the current results from surface generation and $I_2 \approx I_3$. The reverse current is intrinsically small, hence large area diodes are suitable for measuring the excess currents ($I_3 - I_4$).

More importantly, carrier generation can also occur at the film–BOX interface [24]. According to the back-gate bias V_{BG}, the $I_R(V_{FG})$ curves are more (V_{BG} > 3 V) or less (V_{BG} < 3 V) distorted, as shown in Fig. 4c. Consider the case of V_{BG} = 5 V when the back interface is not depleted initially at V_{FG} < 1 V (since body doping N_A is high). As V_{FG} increases, the threshold voltage of the back channel is gradually lowered and the interface becomes eventually depleted, starting to generate carriers. The valley (point V in Fig. 4c) indicates the formation of the front inversion channel and is immediately followed by the depletion of the back interface. The sudden current increase represents the contribution of the back-surface generation velocity.

Reciprocal experiments can be performed by reversing the roles of the two gates, that is monitoring the leakage current as a function of back bias $I_R(V_{BG})$ [24]. In ultrathin FDSOI, carrier generation at the front and back interfaces dominates. Their contributions are hard to discriminate due to carrier inversion that takes place in the whole film volume.

2.3.2. Forward current

It is well known that at relatively low forward voltage ($V_A \approx$ 0.2–0.4 V, lower than the junction build-in voltage, V_K grounded), the diode current is due to the recombination of excess carriers. The profiles of electrons and holes are rather flat along the longitudinal direction from source to drain. We consider the simple

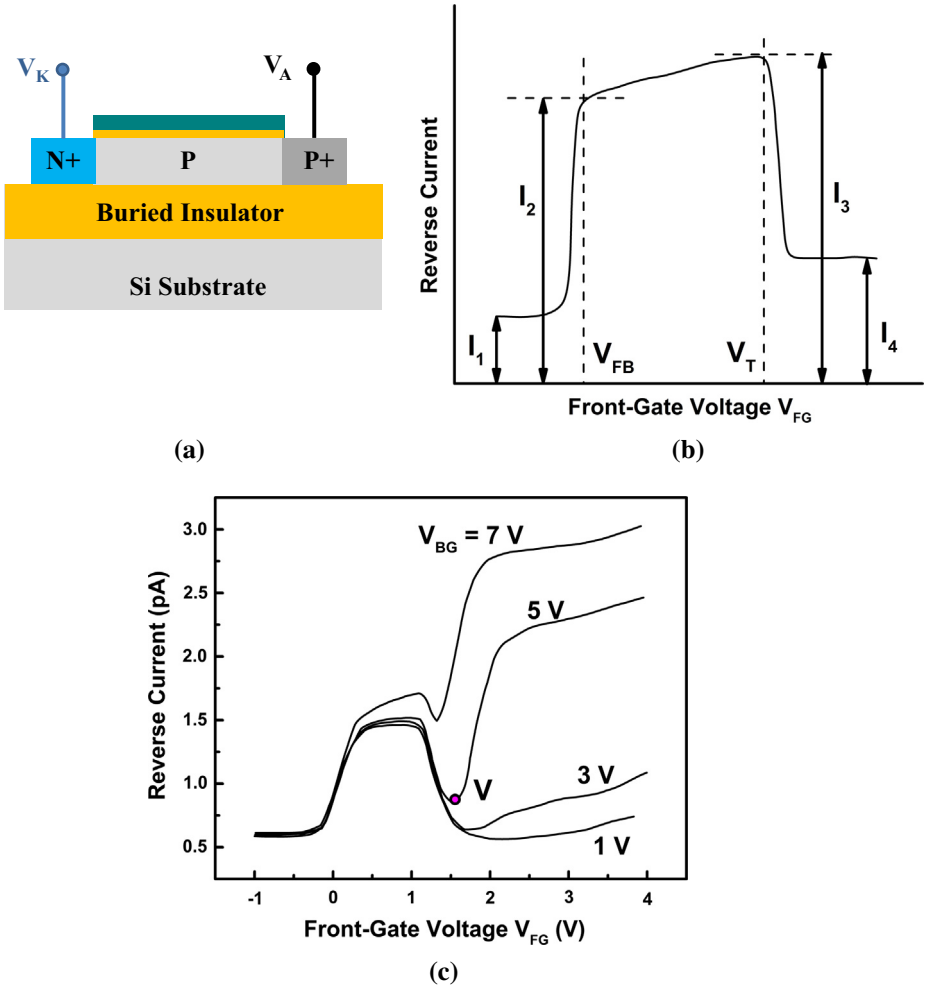

Fig. 4. (a) Schematics of current measurement in FDSOI gated diodes. (b) Generic variation of the reverse current with front-gate bias. (c) Reverse current versus front-gate voltage for various back-gate voltages in SOI gated diodes: V_K = 0.6 V (V_A grounded), W = 240 μm, L = 4 μm, body doping $N_A = 10^{17}$ cm^{-3}, t_{Si} = 150 nm (adapted from [24]).

case of a long diode biased in double-gate mode, which occurs naturally in FinFETs and gate-all-around (GAA) nanowires. In a planar FDSOI diode, the two gates are biased such as to ensure identical potentials at the front and back interfaces [25]:

$$V_{FG} - V_{TF} = \frac{t_{OX}}{t_{BOX}} \cdot (V_{BG} - V_{TB}) \tag{14}$$

If the film is ultrathin, the potential profile is equally quasi-flat in the vertical direction, which means that the carrier concentrations are constant in the whole body volume.

The forward current, measured as a function of gate bias, exhibits a clear peak value (Fig. 5a). Maximum recombination occurs when the concentrations of electrons and holes become equal ($n = p \gg n_i$). In this situation, the quasi-Fermi levels are equidistant from the mid-gap and separated by qV_A. The recombination rate reduces to $R_{max} = n/\tau_r$ and the excess peak current ΔI_F is obtained by simply multiplying R_{max} by the volume of the body which acts as a 'recombination box' [26,27]:

$$\Delta I_F = \frac{qn_i}{\tau_r} \cdot \exp\left(\frac{qV_A}{2kT}\right) \cdot (L \cdot W \cdot t_{Si}) \tag{15}$$

The effective recombination lifetime τ_{eff} includes contributions from volume (τ_r) and interfaces ($S_{1,2}$):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_r} + \frac{S_1 + S_2}{t_{Si}} \tag{16}$$

In relatively thick (100 nm) and high quality SOI the surface recombination can be neglected and the lifetime reaches 0.1 μs [24]. This is not necessarily the case in sub-10 nm thick SOI films where the lifetime extracted from Fig. 5a is much lower (10 ns) showing a notable contribution of the interfaces.

A more sophisticated variant consists in biasing independently the two gates which results in very complicated multiple-peak characteristics, as shown in Fig. 5b [27,28]. The advantage is that the surface velocities $S_{1,2}$ can in principle be determined separately.

2.3.3. Capacitance

Advanced and multipurpose characterization techniques are based on *CV* measurements with SOI gated p–i–n diode. A large variety of parameters can be extracted (front- and back-gate threshold voltage, layer thicknesses and interface traps [29–31]). The main advantage of using a gated p–i–n diode resides in the availability of both electron and hole reservoirs in the same device. These reservoirs enable a simultaneous characterization of n- and p-type MOSFETs since a single capacitance curve provides information on both devices. They also prevent the appearance of out of equilibrium phenomena like the deep depletion regime and/or the impossibility to reach stable capacitance value in accumulation regime. This drawback is usually observed in SOI MOSFET capacitance measurements, when pulsing/sweeping rapidly the gate bias

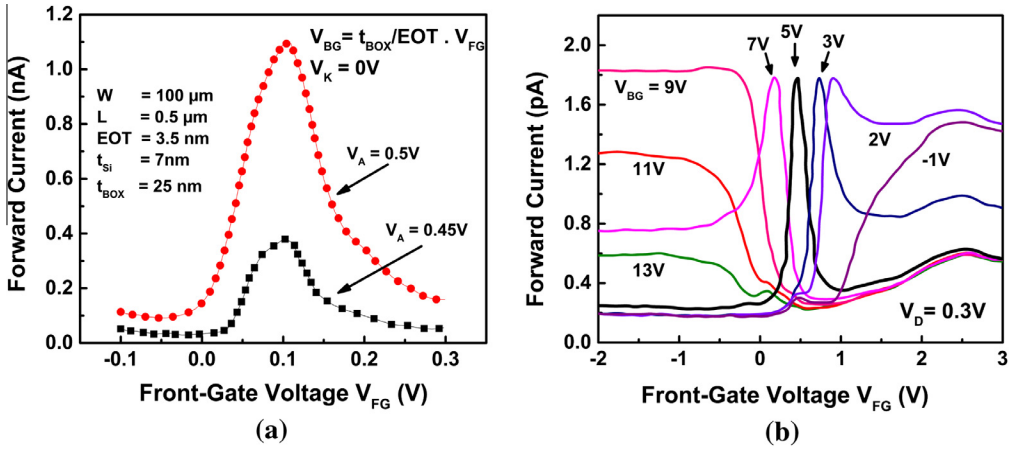

Fig. 5. Experimental forward current versus gate voltage in p–i–n gated diodes. (a) FDSOI diode operated in double-gate mode at various drain biases (courtesy of C. Navarro). (b) Standard SOI diode for various back-gate voltages (V_A = 0.3 V, $W = L$ = 3 µm, adapted from [27]).

into accumulation and/or at high-frequency regime, since the majority carriers are not provided instantly.

Typical capacitance curves in gated diodes are reproduced in Fig. 6a. As V_{FG} is swept from negative to positive bias, the capacitance decreases from the accumulation value, which corresponds to C_{OX}, to a minimum and then increases to the inversion value (again C_{OX}). The minimum capacitance depends on the back-gate bias:

- For V_{BG} = +6 V, the back interface is inverted and the capacitance minimum represents the series combination of front-oxide capacitance and depleted film capacitance ($C_{Si} = \varepsilon_{Si}/t_{Si}$).
- For V_{BG} = 0 V, the bottom interface is depleted and the minimum capacitance is lowered because it includes the contribution of the BOX capacitance and Si substrate.
- For V_{BG} = −2 V, an inflection point occurs and indicates the temporary existence of the back hole channel.

Detailed information is obtained by plotting the capacitance derivative [31]. When sweeping the front-gate voltage, the capacitance derivative exhibits two main peaks that provide simultaneously the front-threshold voltages of n- and p-MOSFETs (Fig. 6b). The threshold voltages extracted by capacitance measurement on p–i–n diodes and by the second derivative on regular MOSFETs are identical simply because the methods are equivalent: $dC/dV_G = d^2Q_{inv}/dV_G^2 \approx d^2I_D/dV_G^2$.

Beyond the advantage of fast extraction using a single device, one can further use the back-gate action. The lateral shift in V_T highlights the displacement of the charge centroid induced by the back-gate bias. For an intermediate bias (V_{BG} = −2 V in Fig. 6b), a third peak appears for V_{FG} = 0.25 V and indicates the transition from strong hole accumulation to depletion at the back channel. In other words, the back threshold voltage of the p-channel MOSFET is −2 V when the front-gate bias is 0.25 V. These details, fully confirmed by numerical simulations, cannot be captured by usual current-based methods (*Y*-function and McLarty), revealing another advantage of the capacitance derivative procedure.

Several current-based MOSFET techniques (*Y*-function, constant current and current extrapolation) have been benchmarked with the capacitive derivative for the front-channel threshold voltage V_{TF} extraction (Fig. 7). This study revealed that when the back channel is depleted or accumulated all $V_{TF}(V_{BG})$ curves are superposed whatever the extraction method. However, when the back channel becomes also inverted, only the p–i–n diode capacitance derivative and the second derivative of drain current exhibit the

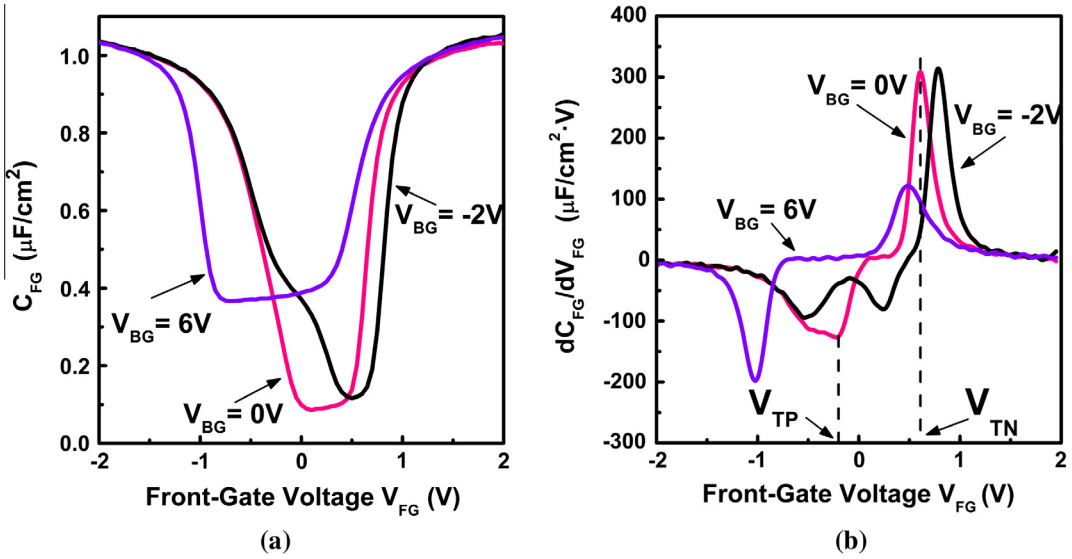

Fig. 6. (a) Split *C*–*V* measurements on 25 nm thick Si-film FDSOI p–i–n gated diodes and (b) capacitance derivative. Example of threshold voltage determination for V_{BG} = 0 V by using the negative (p-MOSFET) and positive (n-MOSFET) peaks in the capacitance derivative [31].

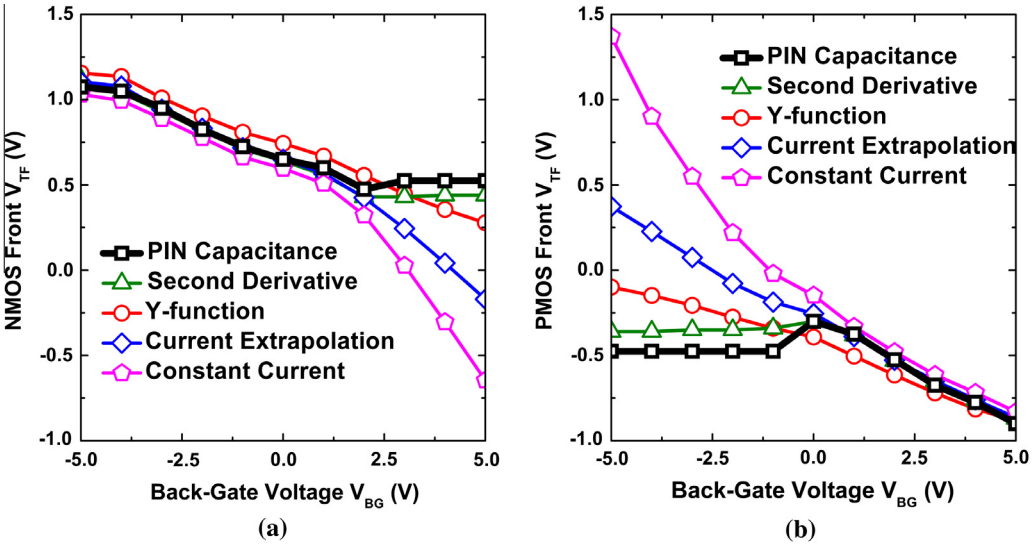

Fig. 7. Threshold voltage comparison between the capacitance derivative method on p–i–n gated diodes and traditional current-based techniques for 25 nm thick Si-film (a) n-channel and (b) p-channel.

expected plateau for V_{TF} [32]. This plateau is mainly induced by the inversion channel at the back interface that screens the impact of the back-gate bias on the front-channel.

Split C–V measurements on p–i–n gated diodes allow also extracting the thicknesses of ultra-thin Si layers (<10 nm) with remarkable accuracy (<0.5 nm). The normal capacitance technique for thickness extraction in MOS transistors or diodes requires the back channel to be strongly inverted (for example V_{BG} = +6 V in Fig. 6a) or accumulated. The minimum capacitance provides C_{OX} in series with C_{Si}. Knowing the front gate-oxide thickness t_{OX} (from C_{OX}), the Si-film thickness t_{Si} can be determined.

Nevertheless, in ultrathin films (t_{Si} < 10 nm), there is no separation between the front and back channels due to the volume inversion [7] and supercoupling [33]. Indeed, it is not possible to strongly invert or accumulate only the back-channel without having a notable impact of the front-gate bias V_{FG}. This means that no accurate capacitance minimum value can be obtained even when a high positive or negative voltage is applied to the back gate.

To overcome this issue, the capacitance derivative is used since it emphasizes the transition from accumulation (or inversion) into depletion at the back interface. A back bias able to induce the hump reflecting the transition from back depletion to inversion is

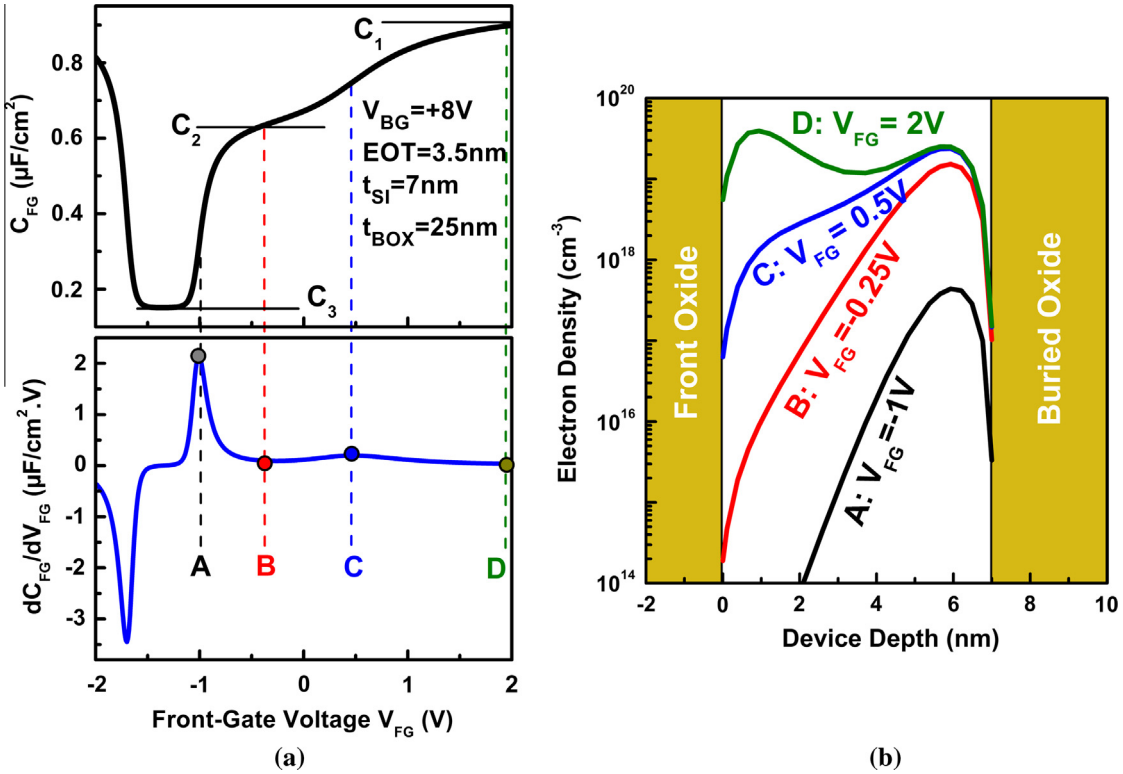

Fig. 8. Simulated (a) capacitance and derivative used for the extraction of the Si-film thickness and (b) vertical doping profiles at points A, B, C and D for V_{BG} = +8 V. Location of point B defines the V_{FG} where the capacitance C_2 is measured for extracting t_{Si}. Ultrathin Si-film diode with L = 0.3 μm and W = 1 μm [31].

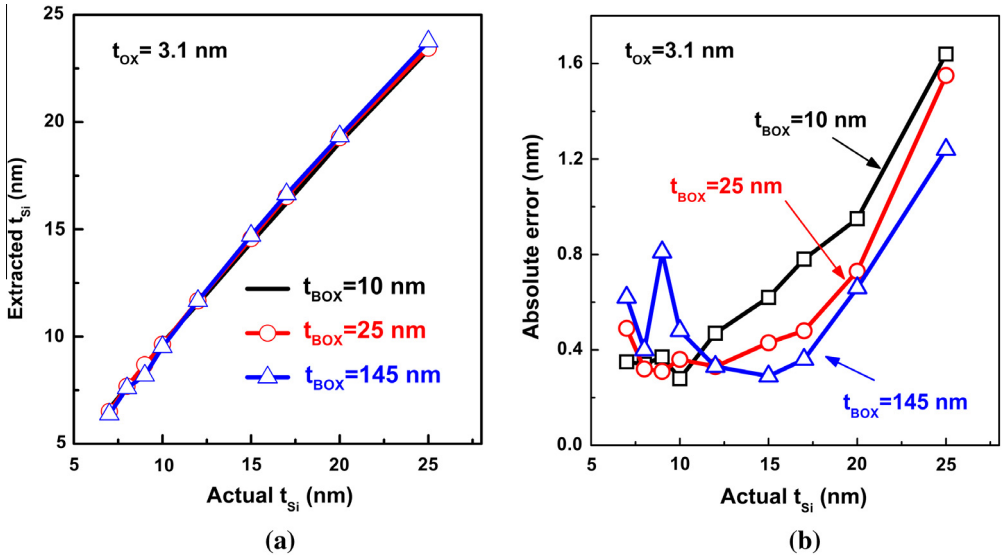

Fig. 9. Simulated (a) Si-film thickness extracted by employing the capacitance derivative on p–i–n gated diodes for several BOX thicknesses and (b) absolute error [28].

required (Fig. 8a). The transition points between the operation regimes are highlighted in Fig. 8a and the corresponding vertical electron concentration profiles are illustrated in Fig. 8b. Points A and C show the formation of the electron back-channel and front-channel ($V_{TF,B}$), respectively. Point D depicts the point where the device accommodates volume inversion and both interfaces are strongly populated with electrons. The point of interest, *B*, denotes the case where the electron concentration at the back-interface is maximum and the front-interface is depleted. The capacitance C_2 at point B provides C_{OX} in series with C_{Si} in ultrathin devices. Fig. 9 shows that this method delivers t_{Si} with an uncertainty limited to only 1–2 monolayers.

2.3.4. Charge pumping

Charge pumping (CP) serves to measure the concentration of interface traps. The principle of CP is to repeatedly switch the gate from inversion to accumulation and vice-versa, which results in an average body current [34]. The P^+ terminal supplies the majority carriers, replacing the body contact of five-terminal MOSFETs. The N^+ contact controls the charge of the inversion layer and can be more or less reverse-biased [35].

In inversion, some of the minority carriers pumped from the N^+ terminal are trapped by the interface states. During the transition from inversion to accumulation, only the mobile electrons of the inversion layer are collected by the N^+ contact before the majority carriers, flowing from the P^+ contact, reach the interface. The recombination of the electrons trapped on the interface states with majority carriers gives rise to a CP current I_{CP} that is proportional to the average concentration of interface traps D_{it} and frequency f:

$$I_{CP} = q^2 \cdot f \cdot D_{it} \cdot \Delta\Psi_s \cdot W \cdot L \tag{17}$$

$\Delta\Psi_s$ is the surface potential range (<1 V) swept through during the gate pulse ΔV_G [34]:

$$\Delta\Psi_s = \frac{2kT}{q} \ln\left(v_{th} \cdot n_i \cdot \sqrt{\sigma_n \cdot \sigma_p} \cdot \sqrt{t_r \cdot t_f} \cdot \frac{|V_{FB} - V_T|}{|\Delta V_G|}\right) \tag{18}$$

where v_{th} is the thermal velocity of carriers, $t_{r,f}$ are the rise/fall times of the trapezoidal ΔV_G pulse and $\sigma_{n,p}$ are the capture cross sections.

As shown in Fig. 10a, the $I_{CP}(f)$ curves are linear over several decades. D_{it} is determined from the slope with Eq. (17).

A common CP variant consists in varying the bottom level V_{GL} of the trapezoidal pulse while keeping the pulse magnitude ΔV_G and frequency fixed (Fig. 10b). The resulting curve is rectangle-like, similar to that of the reverse diode current (Fig. 4b). There are three distinct regions [34,35]:

- *(left)* as long as the top level of the pulse does not reach the threshold voltage, no carrier inversion and no trapping occur, so $I_{CP} \approx 0$;
- *(center)* a maximum CP current (Eq. (17)) is measured when the top level exceeds V_T;
- *(right)* for higher V_{GL} values exceeding the flatband voltage, the surface does not return in accumulation, hence the electron-hole recombination is inhibited and I_{CP} drops to zero.

The left- and right-hand edges of the curve, defined at mid-height, yield $(V_T - \Delta V_G)$ and V_{FB}, respectively. The plateau level gives D_{it} according to Eq. (17).

Fig. 10c shows that increasing the reverse bias V_R reduces the width and height of the plateau because (i) V_T increases and (ii) the junction depletion region expands laterally enabling fewer traps to be pumped. The latter effect is used to evaluate the lateral trap profile along the interface [35,24].

Expert-level measurements, performed by varying the fall and rise time of the pulse, are aimed at evaluating the capture cross-section and the energy distribution of the traps within the bandgap [34]. While very sharp pulses enable to scan the traps located closer to band edges, caution is needed to avoid parasitic recombination. For example, if the fall time is too short, the mobile electrons cannot be collected by the N^+ contact before the arrival of holes. Similarly, for very sharp rise time, the electrons will fill the body before the holes are swept away. Such parasitic electron-hole recombination is accentuated in long diodes and leads to undesirable overestimation of I_{CP} current [35]. Conversely, I_{CP} is underestimated at very high frequency due to the incomplete filling of the interface traps; this is why the time during which the surface is in inversion should be longer than the trapping time constant. A safe approach is to set the time constants of the ΔV_G pulse longer than those of the channel formation and carrier trapping/emission mechanisms.

The modification of the pulse shape (triple-level or triangular) and frequency gives insight on the trapping process and trap

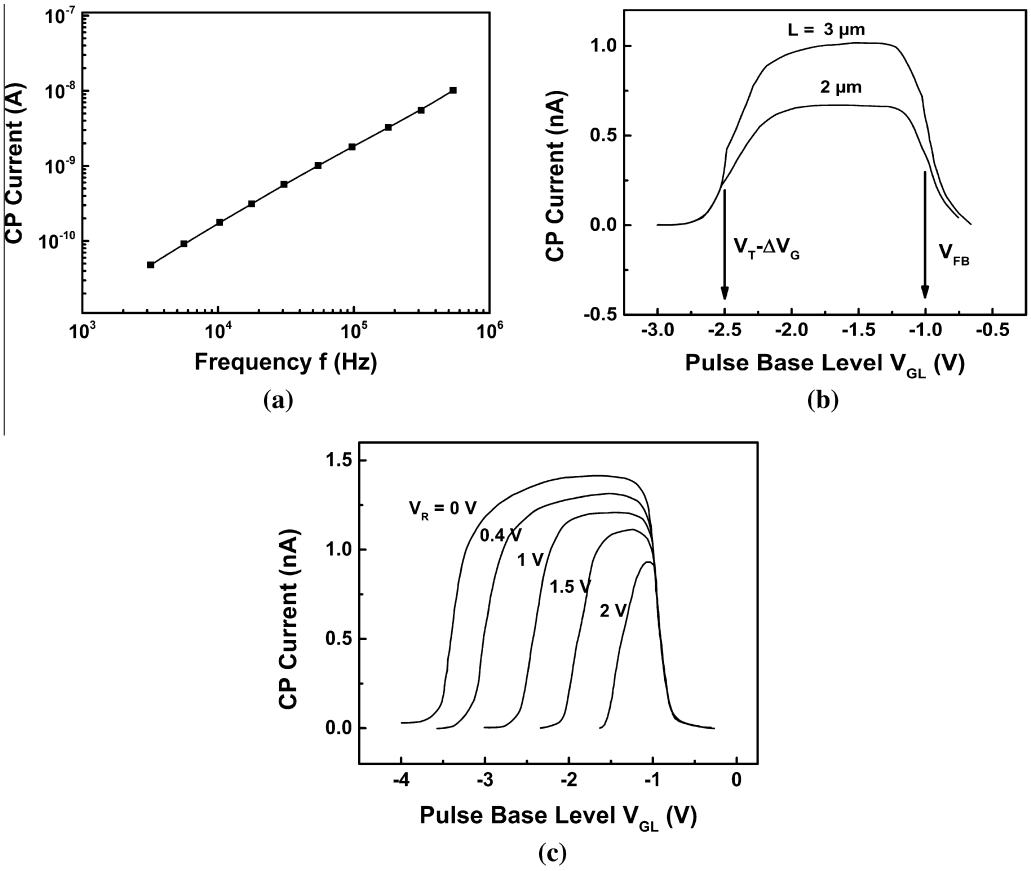

Fig. 10. Charge pumping current versus (a) frequency and (b) base level of the pulse in FDSOI gated diode (L = 2 μm, V_R = 0, ΔV_G = 5 V, $t_r = t_f$ = 100 ns; adapted from [35]). (c) Modification of the CP curve by increasing the diode reverse bias. Adapted from [24].

distribution within the oxide [36]. In ultra-small area devices, the dynamics of individual traps could be identified [37].

The back-gate bias modifies remarkably the CP signature in FDSOI diodes. As documented in Fig. 11a, an excess I_{CP} current is measured in the bias range where the back interface is depleted. Fig. 11b shows the lateral shift of the rectangle-like curve which reflects the modification of the threshold and flatband voltages with V_{BG}. The plateau level is roughly constant for inversion and accumulation at the film–BOX interface and clearly increases for depletion ($V_{BG} = -4$ V). These results indicate that pulsing the front gate induces also the pumping of back interface traps [35]. The difference between I_{CP} values measured with the back channel in depletion or in accumulation has been used to evaluate the D_{it} at the back interface [38].

This comparison does not work any longer in ultrathin FDSOI where the back-surface potential follows the front potential and cannot be maintained in accumulation. CP measurements in sub-10 nm thick SOI devices are governed by the combined effects of front and back traps. It is not clear how they can be discriminated. Nevertheless, CP is a method of choice that offers excellent sensitivity due to the frequency-induced internal amplification.

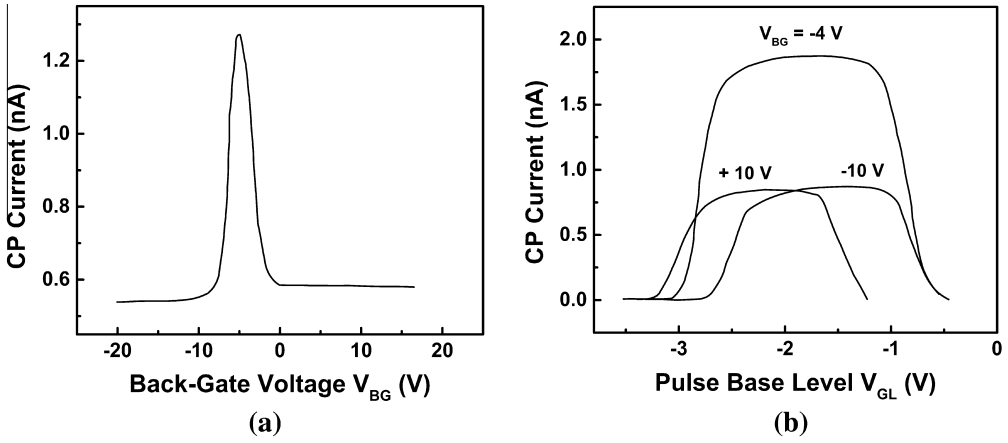

Fig. 11. (a) Charge pumping current measured by pulsing the front gate versus back-gate voltage. (b) Modification of the CP curve for various back-gate biases. Adapted from [24].

2.4. Special methods for MOSFETs

2.4.1. Low-frequency noise

Noise is a powerful tool for the evaluation of oxide, interface and semiconductor traps. It is defined as the power spectral density $S_I(f)$ of the time-dependent drain current fluctuations.

At low frequency, the noise in MOSFETs has a $1/f^{\gamma}$ dependence with $0.8 < \gamma < 1.2$ (Fig. 12a). This *flicker* ($1/f$) noise originates essentially from fluctuations in carrier number via trapping in slow oxide traps located in the dielectric (border traps) [39]. Mobility fluctuations, induced for example by carrier Coulomb scattering near the interface, may also generate $1/f$ noise. The normalized flicker noise is expressed as [40]:

$$\frac{S_I}{I_D^2} = q^2 \cdot kT \cdot \frac{\lambda \cdot N_t}{W \cdot L \cdot f \cdot C_{OX}^2} \cdot \left(\frac{g_m}{I_D}\right)^2 \cdot \left(1 + \alpha \cdot \mu_{eff} \cdot C_{OX} \cdot \frac{I_D}{g_m}\right)^2 \quad (19)$$

where N_t is the slow trap density, λ is the tunneling constant ($\sim$0.1 nm), μ_{eff} is the effective mobility and α is the Coulomb scattering coefficient. When the latter term is negligible, the variations of S_I/I_D^2 and $(g_m/I_D)^2$ are proportional to each other.

Typical noise curves in FDSOI MOSFETs are shown in Fig. 12b. In weak inversion, mobility fluctuations are negligible ($\alpha = 0$) and the normalized $1/f$ noise S_I/I_D^2 is constant. The density of traps is determined from the plateau level with Eq. (19). In strong inversion the noise level decreases rapidly, roughly as $\sim 1/(V_G - V_T)^2$. The presence of mobility fluctuations due to Coulomb scattering is detected from the difference between S_I/I_D^2 and $(g_m/I_D)^2$ curves.

When several sources of noise coexist, their contributions are added and lead to more complicated characteristics [41–43]. This is the case of FDSOI MOSFETs where noise can be generated at both the front and back interfaces. The discrimination of noise sources is possible by measuring the noise of each channel for various biases applied on the opposite gate. As a result, the noise curve is modified in two respects (Fig. 12c): additional noise generated at the opposite interface and change of the surface potential at the probed channel.

This strategy has demonstrated that, in 28 nm and 14 nm FDSOI technology nodes, the density of slow traps in the BOX ($3.5 \cdot 10^{17}$ $cm^{-3}eV^{-1}$) is consistently lower than in the high-k gate dielectric ($9 \cdot 10^{17}$ cm^{-3} eV^{-1}) [41]. Mobility fluctuations were observed only at the front channel and they increase significantly as the body becomes thinner. Generation–recombination noise with $1/f^2$ spectrum was equally detected in short MOSFETs and attributed to defects resulting from the processing of source/drain terminals [41].

In small area transistors, where only few traps exist, single-carrier trapping gives rise to *Random Telegraph Noise* (RTN), meaning that small pulses are superimposed on the average current (Fig. 12d). The duration and signature of RTN signals is used to determine the trapping/emission time constants of the trap. RTN is typical in FDSOI TFETs (tunneling field-effect transistors) where only a discrete number of traps are influential even in a large-area device. This is so because the tunneling junction is very narrow ($\sim$10 nm) and experiences few trapping events [44].

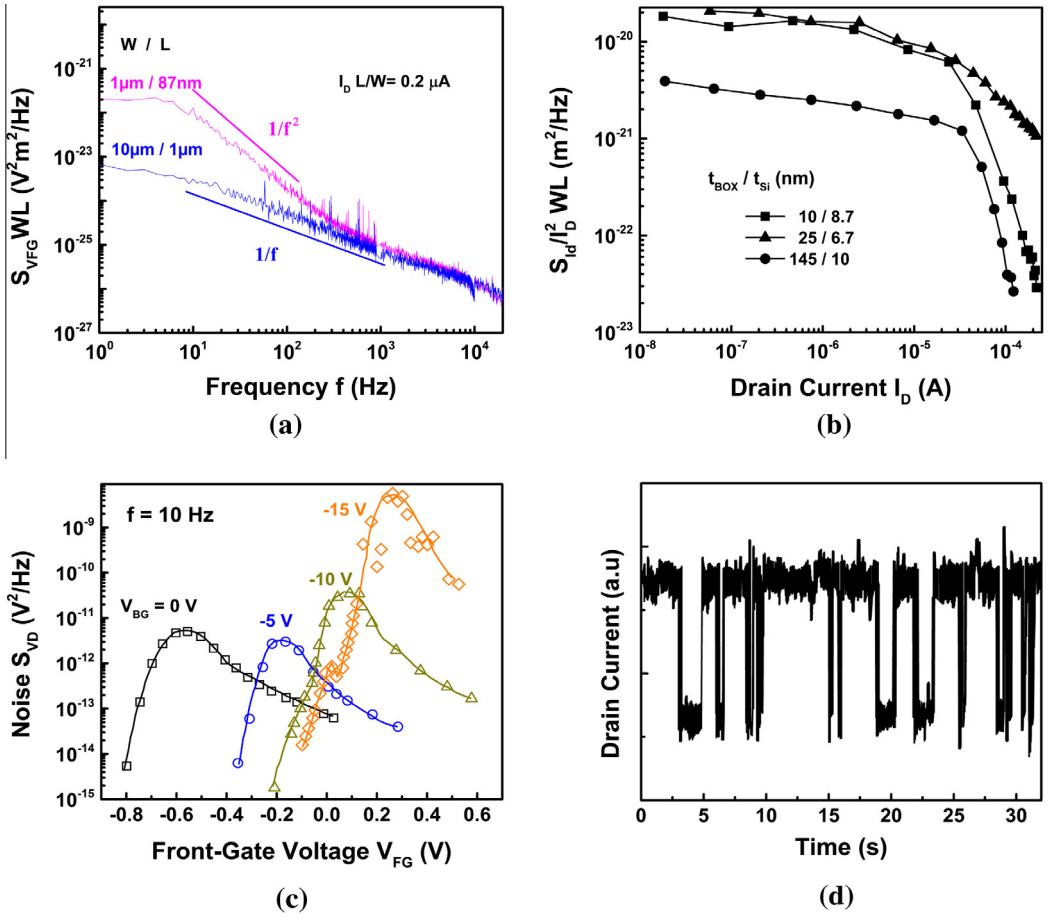

Fig. 12. (a) Noise spectra in 14 nm FDSOI MOSFETs showing flicker $1/f$ noise and additional generation–recombination $1/f^2$ noise in short channels [41]. (b) Normalized drain current noise factor versus drain current (f = 10 Hz, 14 nm FDSOI) [41]. (c) Front channel noise curves for various back biases showing strong coupling effects [42]. (d) RTN signals in small FDSOI MOSFETs.

2.4.2. Geometric magnetoresistance

The geometrical magnetoresistance (MR) is the most accurate and indisputable method to determine the carrier mobility in short MOSFETs, where lateral Hall contacts cannot be implemented. The technique consists in measuring the decrease of drain current under high magnetic field.

This peculiar magnetoresistance arises from the duality of Hall and MR effects. Under vertical magnetic field B_z field and longitudinal electric field E_x, the Lorentz force $\vec{F} = q\vec{v} \times \vec{B}$ tends to deviate the channel carriers in the lateral direction (y). The higher the carrier velocity v (i.e., mobility), the stronger the deviation. In long samples (Fig. 13a), the Hall field opposes the Lorentz force and the carriers follow the electric field between the two electrodes without seeing the magnetic field. The MR is therefore weak and simply reflects the carrier energy distribution. But, if the Hall effect is prevented to develop, the Lorentz force does deflect the carriers. Their trajectory takes a circular path, interrupted by scattering events, which is longer than the channel length; hence the resistance of the sample increases. This effect, named geometrical MR, is typical for Corbino disks where the circular geometry of the sample inhibits the Hall effect. MR measurements can be performed on Pseudo-MOSFET with Corbino configuration [45] as shown in Fig. 16b.

Very short and wide samples (Fig. 13b) mimic the Corbino geometry. Indeed, the end contacts impose the potential value on the sidewalls and short-circuit the Hall voltage [46,47]. In practice, for MOSFETs with large aspect ratio ($W/L > 10$), the Hall field is effectively suppressed leading to a maximum 'geometrical' MR [47–51]:

$$R_B = R_0 \cdot (1 + \mu_{MR}^2 \cdot B^2) \tag{20}$$

where $R_{0,B} = V_D/I_D$ is the channel resistance measured at zero or at high magnetic field and μ_{MR} is the magnetoresistance mobility.

The MR method is straightforward: the $I_D(V_G)$ characteristics in the ohmic region are recorded as a function of field (Fig. 13c) and the ratio R_B/R_0 is plotted against the squared magnetic field. A straight line is obtained (Fig. 14a), the slope of which yields μ_{MR}.

The universal Eq. (20) is valid from weak to strong inversion and for any combination of gate biases. More importantly unlike the other mobility characterization methods, the MR is free from approximations regarding the device architecture, oxide and film thickness, gate stack, effective dimensions, doping, strain, etc. It follows that the MR mobility is a genuine and valuable parameter for the investigation of the carrier transport in MOSFETs.

Compared to the drift mobility, which is proportional to the mean relaxation time $\mu \sim \langle \tau \rangle$, the MR mobility varies as

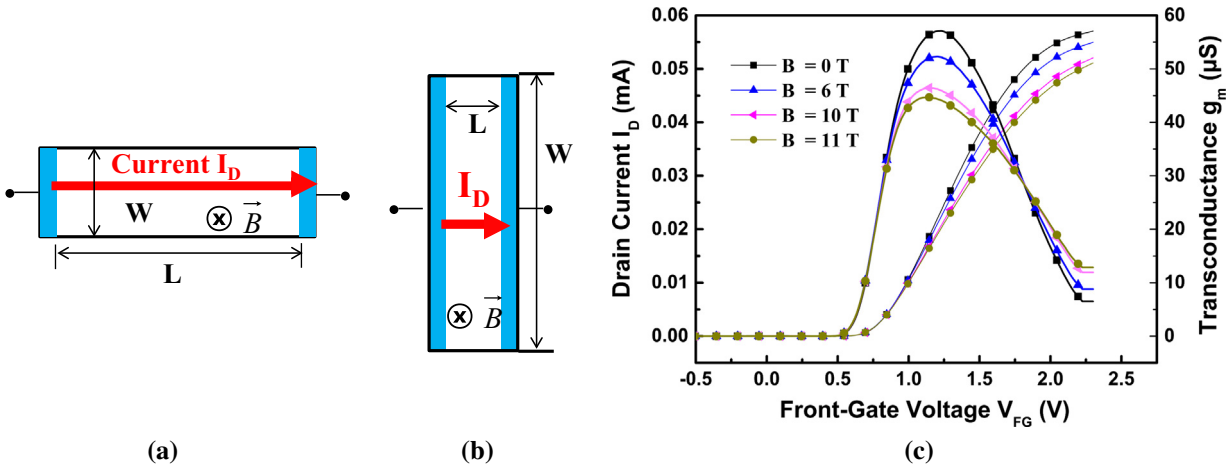

Fig. 13. (a) Long sample under magnetic field: maximum Hall effect and negligible MR. (b) Short and wide sample: no Hall effect, maximum geometric MR. (c) Modification of drain current $I_D(V_{FG})$ and transconductance $g_m(V_{FG})$ characteristics under high magnetic field. FDSOI MOSFET with L = 1 μm, W = 10 μm, V_D = 10 mV, T = 100 K (adapted from Chang et al. [51]).

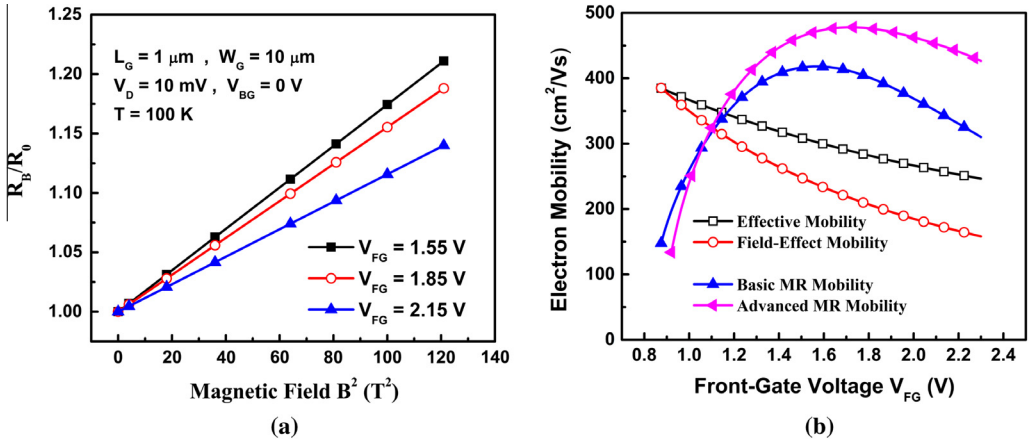

Fig. 14. (a) Normalized geometrical MR versus squared magnetic field. The MR mobility is extracted from the slope for each gate bias. (b) Electron mobility versus gate voltage as determined by different methods: field-effect mobility from transconductance, effective mobility from Y-function, MR mobility from Eq. (20), corrected MR mobility by accounting for series resistance effects (Eq. (21)). Same device as in Fig. 13c.

$\mu_{MR} \sim (\langle\tau^3\rangle/\langle\tau\rangle)^{0.5}$ [47,50]. This is why the MR mobility is higher than the drift mobility by a factor of 1.1–2 which depends on the type of scattering mechanism [50].

The lone requirement is to utilize high magnetic field ($B \sim 1/\mu$) such as to obtain a measurable MR effect. Typical measurements in FDSOI MOSFET are shown in Fig. 13c [51]. At high magnetic field, the drain current and transconductance peak clearly decrease, whereas the threshold voltage and subthreshold slope are hardly affected.

Short-channel FDSOI MOSFETs are prone to large series resistances R_S. The variation of R_S under magnetic field can be ignored because the mobility in the heavily doped source and drain terminals is modest. The total measured resistance is $R_B = R_S + R_0 \cdot (1 + \mu_{MR}^2 \cdot B^2)$, leading to a simple modification of Eq. (20):

$$\frac{R_B}{R_0} = 1 + \frac{R_C}{R_S + R_C} \cdot \mu_{MR}^2 \cdot B^2 \tag{21}$$

where R_C is the channel resistance and R_S can be measured independently (see Section 2.1.1).

In Fig. 14b, the MR mobilities calculated with Eqs. (20) and (21) are compared with the effective mobility and field-effect mobility (reconstructed using the *Y*-function, Section 2.1.1). The latter mobilities are valid only in strong inversion, which explains the difference in shape with the MR mobility. The MR mobility dependence on gate voltage is bell-shaped and the two sides correspond to moderate and strong inversion. At low gate voltage, the electron mobility is dominated by (remote) Coulomb scattering on ionized centers (primarily HfO_2 defects rather than body dopants), which are gradually screened by the formation of the strong inversion layer. After a maximum is reached, the mobility decreases due to higher vertical electric field. As expected, the effective mobility is higher than the field-effect mobility μ_{FE} (which overestimates the vertical field dependence) and smaller than μ_{MR}.

2.4.3. Drain current transients

An excess or deficit of majority carriers in the floating body cannot be compensated instantly (no body contact) which leads to transients in body potential, drain current and gate current [9,52,53]. Equilibrium is reached by carrier recombination–generation, junction leakage and band-to-band tunneling (BTBT).

A typical experiment in FDSOI MOSFET consists in pulsing the front gate from depletion into accumulation (V_{FG}: $0 \rightarrow -1.5$ V in Fig. 15), while the back gate is maintained in inversion. Since no holes are available, the body potential drops by capacitive coupling, suddenly increasing V_{T2} and lowering (or canceling) the drain current. The drain current I_0 relaxes back to equilibrium (undershoot) through carrier *generation* (Fig. 15). Models are available for extracting the effective generation lifetime with Zerbst-like techniques [54].

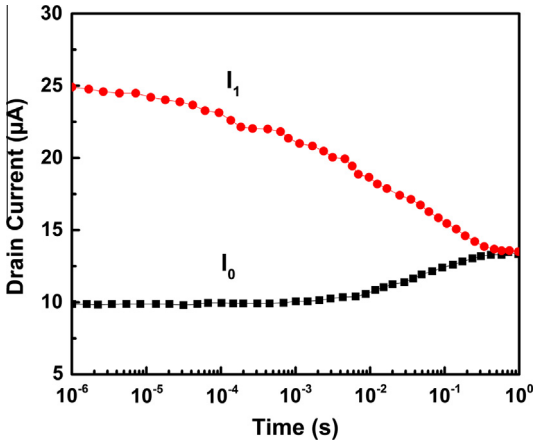

Fig. 15. Drain current transients in FDSOI transistor used as 1T-DRAM. The front gate is pulsed from strong accumulation (−3 V) to moderate accumulation (−1.5 V: current overshoot I_1) or from depletion (0 V) to accumulation (−1.5 V: current undershoot I_0). V_{BG} = 7 V, t_{Si} = 25 nm, EOT = 2.9 nm, t_{BOX} = 25 nm, L = 60 nm.

The opposite case happens when the front gate is pulsed from heavy to moderate accumulation (V_{FG}: −3 V → −1.5 V in Fig. 15). At high negative voltage, BTBT is efficient and supplies holes into the body. The sudden change in V_{FG} leaves the body with more holes than the front gate can accommodate, which means that the potential is higher than at equilibrium. Subsequent carrier *recombination* makes the potential and drain current I_1 decrease (overshoot) to the steady-state values.

The difference in I_1 and I_0 currents is the base of single-transistor dynamic memory (1T-DRAM). This device, also named MSDRAM [55], has the tremendous advantage of not requiring an external storage capacitor as the conventional DRAM does. The current value depends essentially on the back-gate bias in '1'-state and on the V_{FG} pulse in '0'-state. By appropriate biasing, I_0 can be totally suppressed which yields excellent memory margin ($I_1/I_0 > 10^4$). The memory state '1' is permanent whereas state '0' requires refresh. The retention time is defined by the time needed for $I_0(t)$ to reach the equilibrium value (~1 s at 300 K, Fig. 15).

Another consequence of transient mechanism is the 'history' effect. At high-frequency switching of integrated circuits, the transistor body is not able to reach equilibrium rapidly enough; the iterative process of body charging and discharging may be responsible for dynamic instabilities.

3. Characterization of FDSOI materials

The electrical quality of SOI wafers needs to be evaluated before starting the sophisticated and expensive fabrication process of CMOS circuits. In this chapter, we will present the most informative and pragmatic methods, as well as their recent advances. A large part will be dedicated to the pseudo-MOSFET transistor.

3.1. Basic pseudo-MOSFET characterization

The operation of the pseudo-MOSFET lays on the observation that SOI materials mimic an upside-down MOS structure. A voltage applied on the wafer substrate induces electron or hole channels at the film–BOX interface, depending on the voltage polarity. In this configuration, the substrate acts as a back gate, the BOX is the gate dielectric and the Si film is the 'body' of the transistor. Most of the measurements classically used on MOSFETs are adaptable to pseudo-MOSFETs. There are three practical considerations:

- Location of source and drain contacts on the film.
- Nature of the contact between the source/drain probes and film.
- Equivalent width/length aspect ratio (geometrical factor f_g) of the channel.

In practice, these aspects are correlated. The sample geometry is defined by simple lithography and etching to avoid edge leakage current from film to substrate. The three implementations of the measurements are shown in Fig. 16:

1. The standard pseudo-MOSFET (Fig. 16a), in which two metallic probes are placed on the film and used as source and drain [56]. The contact is ohmic thanks to the adjustable pressure of the probes [57]. The geometrical factor $f_g \approx 0.75$ was estimated by comparison between pseudo-MOSFET and 4-probes measurements and further validated by simulations [58]. Note that for ultra-thin films, f_g could be smaller [59].

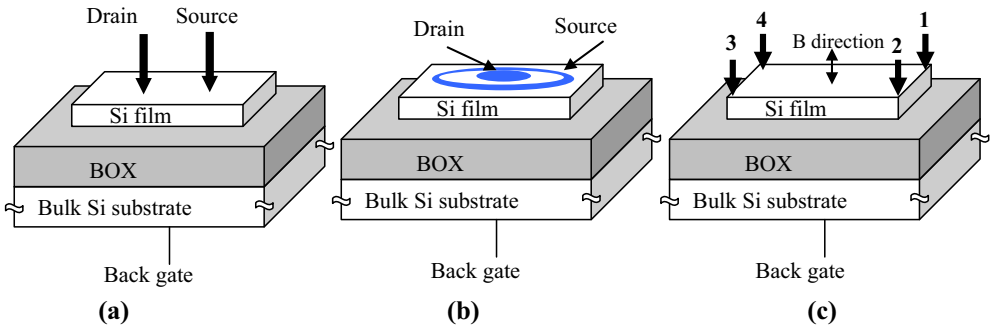

Fig. 16. Different configurations of the samples and contacts used for direct measurement of the SOI material characteristics: (a) pseudo-MOS with pressure probes, (b) pseudo-MOS with circular mercury probes (Hg-FET) or deposited metal contacts and (c) Van der Pauw sample.

2. The Hg-FET, with mercury probes for source and drain (Fig. 16b). The sample has the so-called Corbino geometry where the geometrical factor is analytically defined by the outer and inner radius R_2 and R_1: $f_g = 2\pi/\ln(R_2/R_1)$ [60]. The contact between the film and the Hg probes is typically Schottky-like with a barrier height extremely sensitive to the treatment applied on the film surface before the measurement [61].
3. Pseudo-MOSFET with metal (titanium/aluminum [62] or erbium/silver [45]) ohmic contacts deposited on the film. Such samples with Corbino geometry have served for magnetoresistance measurements.

The easiest structure from the experimental and modeling viewpoints is the one with ohmic pressure contacts. Furthermore, the possibility to test both electrons and holes with the same sample is appealing; therefore we will focus the following discussions on the pseudo-MOSFET.

Ever since its discovery, the pseudo-MOSFET was used for I_D–V_{BG} measurements in order to extract mobility for electrons and holes, D_{it} values, threshold and flatband voltages needed to turn on the channels of electrons and holes, respectively [63]. One of the challenges of the pseudo-MOSFET was the possibility to extend it to very thin films, without damaging the film and/or the BOX integrity. State-of-art ultrathin films down to 12 nm thickness were successfully measured, as showed in Fig. 17a [64]. Fig. 17b, presents the *Y*-function, calculated from the measurements in Fig. 17a, as well as the parameters exacted.

Recent results showed a 4-probes set-up with larger radius probes that induce less damage in the film and enable reliable characterization for ultrathin films and BOX [65]. Several extensions of the pseudo-MOSFET method have been proposed and successfully demonstrated: low-frequency noise [66], geometric magnetoresistance [45], photo-current [67], etc. SOI films down to 40 nm thickness were tested at low temperature with a cryogenic probe station. The mobility dependence on temperature allowed identifying the phonon scattering as the dominant scattering mechanism in the 77–300 K range [68]. Other extensions will be discussed in the next sections.

3.2. Advanced pseudo-MOSFET

3.2.1. Split-CV measurements in pseudo-MOSFET

CV measurements directly on SOI substrates were reported by Li's [69] and Schroder's groups [70]. For example in [70], the MOS capacitors were made on thick or high-resistive SOI wafers with aluminum contacts on top of the film (with or without top gate dielectric). The measurement of the capacitance between the sample surface and the substrate contact is difficult to interpret due to the fully depleted film and the mixing of several interfaces. The split-*CV* method is far more efficient and adaptable to ultrathin FDSOI.

As discussed in Section 2.2, split-CV measurements provide the effective mobility as a function of the applied back-gate bias, inversion charge density or vertical electric field. With the pseudo-MOSFET, the measurements are simply performed using the substrate as a back-gate, connected to the high potential of the impedance-meter, while source and drain probes were connected together to the low potential [71]. A typical experimental

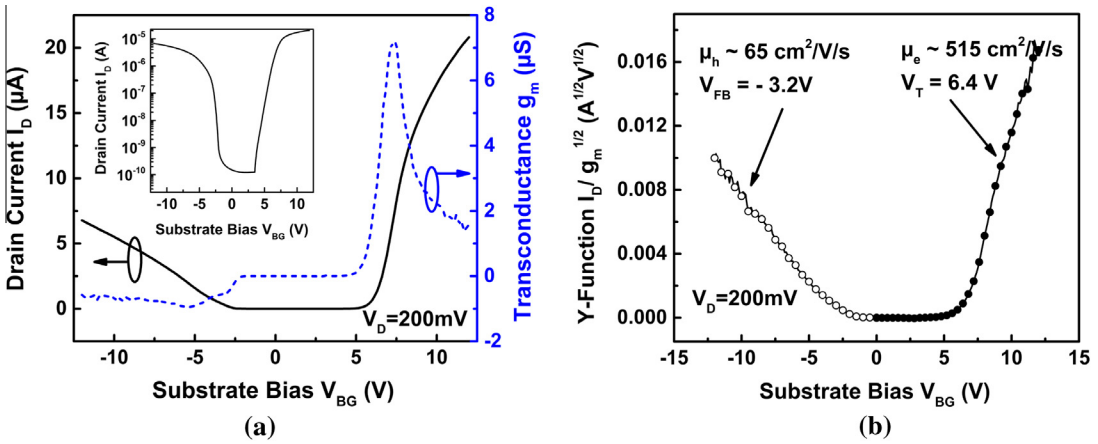

Fig. 17. (a) Drain current and transconductance versus V_{BG} for a passivated SOI wafer with 12 nm film and 25 nm BOX thicknesses. (inset) Curve in semilog scale. (b) Corresponding *Y*-function as well as the extracted mobility, threshold and flatband voltage values (adapted from [64]).

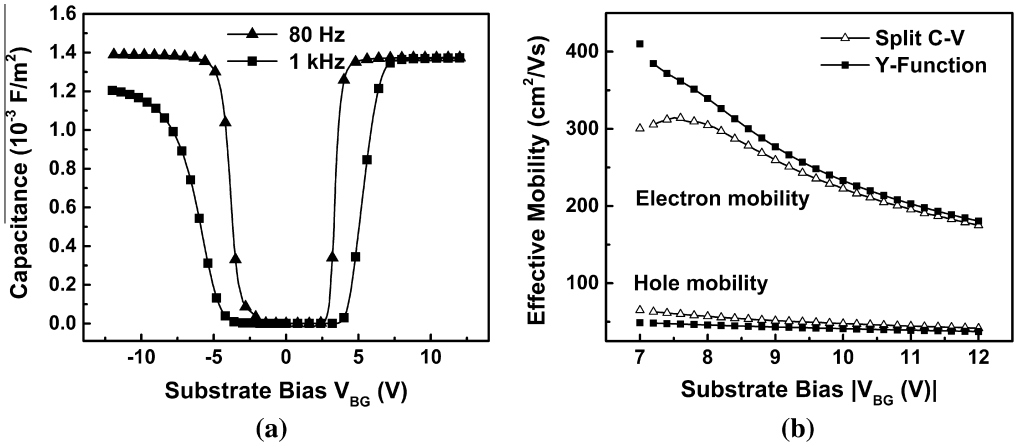

Fig. 18. (a) Typical split capacitance per unit area versus back-gate voltage curve measured on FDSOI in pseudo-MOSFET configuration for 80 Hz and 1 kHz. (b) Effective electron and hole mobility versus back-gate voltage at 130 Hz. The V_{BG} axis is represented in absolute value (negative V_{BG} for holes and positive V_{BG} for electrons). 12 nm film, 25 nm BOX, non-passivated top film. Adapted from [64].

capacitance curve is shown in Fig. 18a, for two signal frequencies. At low frequency (80 Hz in Fig. 18a), the maximum capacitance values, obtained in strong accumulation and strong inversion, are identical and correspond to the BOX capacitance.

Using the procedure explained in Section 2.2, the effective mobility can be extracted for electrons and holes. Fig. 18b shows the effective mobility versus the absolute value of the back-gate voltage. For validation purpose, a 'reference' effective mobility was re-constructed with Eq. (5) from current measurements using the low-field mobility extracted with *Y*-function (full symbols in Fig. 18b). The superposition of the curves in strong inversion proves the ability of the split-*CV* in pseudo-MOSFET to provide reliable effective mobility values.

From the experimental point of view, the quality of the back side contact proved to be critical for split *C*–*V* measurements [72]. A normal 'air' contact leads to a limited capacitance value, while vacuum between the SOI substrate and the chuck allows reaching the expected BOX capacitance. Interestingly, even in case of air-contact between the SOI and the chuck, when the maximum capacitance values are lower than C_{BOX}, accurate effective mobility values can still be obtained thanks to the definition of an 'effective surface' that the BOX thickness and capacitance match [71,73].

When performing these measurements, the choice of the measurement frequency is critical because it can dramatically affect the accuracy. For the effective mobility, low-frequency (<200 Hz) is suitable. At higher frequency, parasitic resistances due to channel creation start to be notable and the maximum capacitance values are decreasing (see for example the 1 kHz curve in Fig. 18a). Using MOS-like theory for charge inversion calculation [74] and for estimation of the access resistance between a probe and any point in the channel [75], a model has been developed that fully explains the frequency dependence [76].

The split-*CV* gives not only a capacitance but also a conductance term. In MOSFETs, conductance versus frequency curves are known to show a peak, the magnitude of which gives D_{it} [18]. This temptation should be refrained in pseudo-MOSFET because the peak, indeed present in the conductance curves, is actually dominated by the channel resistance [76].

3.2.2. Contactless pseudo-MOSFET

Even though 10 nm thick film on 25 nm BOX can still be tested with pressure contacts, the development of contactless methods is foreseen for the next generation substrates. The Second Harmonic Generation (SHG) is such a non-destructive optical technique that already proved its interest for SOI characterization [77,78]. The method is based on the analysis of the intensity of the second harmonic generated in a material, by a high intensity laser. Femtosecond laser pulses of $\lambda \approx 800$ nm wavelength are impinging the wafer surface. A second order polarization term is generated in the material at $\lambda/2$ [79] and the corresponding intensity is measured, as explained in Fig. 19a.

For centro-symmetric materials as silicon or silicon dioxide, the second order susceptibility tensor $\chi^{(2)}$ in the bulk material is zero. Nevertheless, in stacked materials the breaking of the crystallographic symmetry induces non-zero susceptibility tensor components at the interfaces. Furthermore, a supplementary static electric field E_{static} (internal or externally applied to the material) would also generate a second order polarization contribution, depending on the third order susceptibility tensor $\chi^{(3)} \cdot E_{static} \cdot E(\omega) \cdot E(\omega)$; this phenomenon is known as the EFISH (electric field induced second harmonic) [80]. Consequently, the total second harmonic intensity in SOI is given by the sum of the contributions coming from all the interfaces:

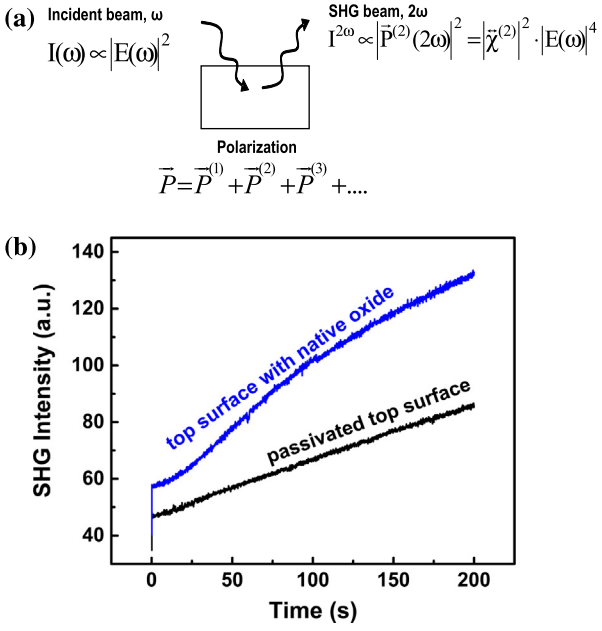

Fig. 19. (a) The principle of SHG. (b) SHG intensity measured on two SOI samples (12 nm film and 25 nm BOX), one with passivated surface and the other with poor quality native oxide.

$$I^{2\omega}(t) \propto \sum_i |\chi_i^{(2)} + \chi_i^{(3)} \cdot E_i(t)|^2 \cdot (I^{\omega})^2 \quad (22)$$

The measurement of the SHG signal at the initial moment (just after shining the laser on the SOI surface) yields the static electric fields at different interfaces, while its time evolution is governed by charging-discharging effects associated to interface and/or oxide traps. An additional effect was tested by Jun et al. [78]: the radiation-induced trapped charges modify the electric field at the interface, leading to an increase in the overall SHG signal.

Fig. 19b shows the SHG intensity measured on FDSOI with 12 nm film and 25 nm BOX. Passivated and non-passivated samples were compared. The initial values of the intensity, as well as the time dependence of the signal are different. This result was expected since it is already known that the passivation improves the top interface state [81], which changes both the internal electric field and the carrier trapping.

SHG can complement the capabilities of the pseudo-MOSFET by replacing the monitoring of the drain current with optical signal measurements. The external electric field resulting from back-gate biasing is well detected by SHG. This means that the SHG signal can be probed as a function of the gate bias (or electric field) and reveals the build-up of the inversion/accumulation charge at the film/BOX interface. Fig. 20 shows the saturated SHG signal versus the back-gate voltage. The shape of the curves clearly reminds the I_D–V_{BG} curve in Section 3.1 and can be used to evaluate electrical parameters (threshold and flatband voltages) by optical means. Furthermore, inductive back-gate biasing is expected to make this method fully contactless.

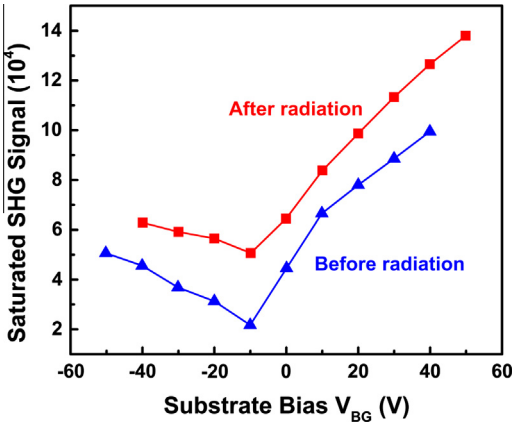

Fig. 20. SHG signal versus back-gate bias before and after radiation with a dose of 5 Mrad. SOI with 72 nm film thickness and 230 nm BOX thickness (adapted from [78]).

3.2.3. Adapted pseudo-MOSFET for highly doped SOI

Highly-doped SOI substrates gained interest after the introduction of junction-less transistors [3] or thanks to the possibility to adjust the threshold voltage. As for any starting material, the characterization strategy needs to be adapted to these highly-doped films, before complete MOS fabrication process.

Fig. 21 shows $I_D(V_{BG})$ and transconductance curves measured in pseudo-MOSFET configuration on 10 nm thick films. Obviously, they are unlike the typical pseudo-MOSFET characteristics obtained on low-doped films (Fig. 17a); therefore the extraction methods cannot be applied directly [82,83]. The first remark is that the drain current is never zero, since no full depletion is achieved in these films because of their heavy doping level ($\sim 10^{20}$ cm^{-3}). Furthermore, the transconductance is quasi-constant (Fig. 21b) suggesting that the current modulation by the back gate is completely different than in low-doped films. The conduction here is mainly due to the dopants whereas the effect of the back gate is only to vary the width W_{SCR} of the depletion region i.e., the size of the conducting channel (t_{Si}–W_{SCR}). In the p-doped film, the depletion is obtained for a positive V_{BG} (case of boron in Fig. 21), while for the n-type film the depletion is induced by a negative V_{BG}.

For this partial depletion mode, the current in a p-type film can be written as:

$$I_D = I_{vol} = f_g \cdot q \cdot \mu_{p,vol} \cdot N_A \cdot (t_{Si} - W_{SCR}) \cdot V_D \quad (23)$$

with f_g the geometry factor, q the electron charge, $\mu_{p,vol}$ the volume mobility, N_A the dopant concentration, and V_D the drain voltage. The V_{BG} dependence is 'hidden' in W_{SCR}, given in first approximation by:

$$W_{SCR} = \frac{C_{BOX}}{q \cdot N_A} \cdot (V_{BG} - V_{FB}) \quad (24)$$

The drain current is then expressed as:

$$I_{vol} = f_g \cdot \mu_{p,vol} \cdot C_{BOX} \cdot (V_{BG} - V_0) \cdot V_D, \text{ with } V_0 = V_{FB} + \frac{q \cdot N_A}{C_{BOX}} \cdot t_{Si} \quad (25)$$

V_0 is the hypothetical voltage necessary to apply on the back gate in order to fully deplete the channel. Of course this voltage cannot be measured in partially depleted films. A simple linear fit of I_D–V_{BG} curve (Fig. 21), yields the volume mobility as well as V_0 from which the doping concentration N_A is extracted.

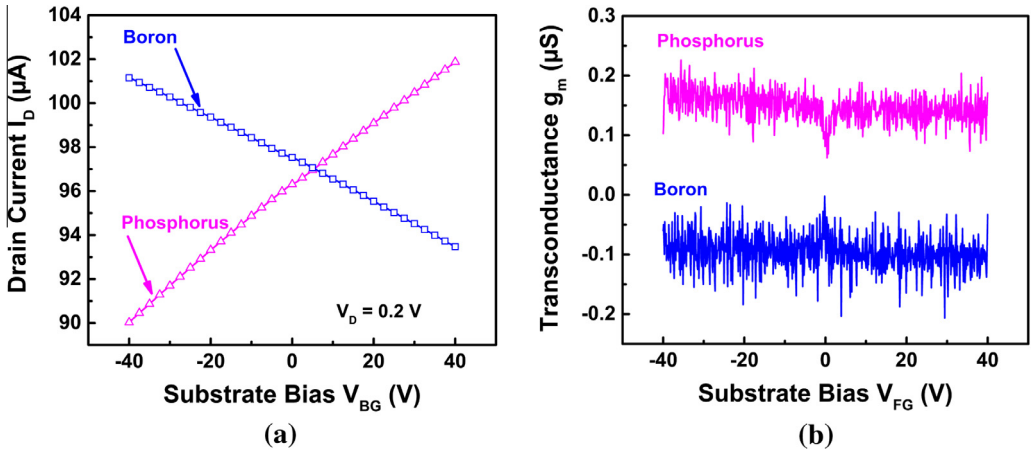

Fig. 21. Drain current (a) and transconductance (b) versus back-gate voltage measured with pseudo-MOSFET in SOI films with 10 nm thickness and 145 nm BOX. The doping levels are about 10^{20} cm^{-3}.

A lower dopant concentration ($\sim 10^{19}$ cm^{-3}) in thicker films (40 nm) produces similar results [82]. However, a supplementary regime is observed when the back-gate voltage induces an accumulation channel at the film–BOX interface; the associated accumulation current adds to the volume current. This contribution is evidenced by a superlinear variation of current for positive V_{BG} in n-type films and for negative V_{BG} in p-type films (Fig. 22a) and by a non-constant transconductance (Fig. 22b). The modeling of this regime is based on the superposition of the volume and the accumulated interface currents:

$$\begin{aligned} I_D &= I_{vol} + I_{acc} \\ &= f_g \cdot q \cdot \mu_{p,vol} \cdot N_A \cdot t_{Si} \cdot V_D \\ &\quad + \left| f_g \cdot C_{OX} \cdot \frac{\mu_{p,surf}}{1 + \theta_{acc} \cdot (V_{BG} - V_{FB})} \cdot (V_{BG} - V_{FB}) \cdot V_D \right| \end{aligned} \tag{26}$$

The contribution of the accumulation channel is isolated by removing from the total current the volume current measured at $V_{BG} \approx V_{FB}$. The classical Y function is redefined to address the accumulation current only (Fig. 22c):

$$Y_{acc} = \frac{I_D - I_{vol}}{\sqrt{g_m}} = \sqrt{f_g \cdot C_{OX} \cdot \mu_{surf} \cdot V_D} \cdot (V_{BG} - V_{FB}) \tag{27}$$

The parameter extraction is done as usual: the mobility in the accumulated channel from the slope and the flatband voltage from the intercept. The mobility values extracted by these methods in both depletion regime and in accumulation regime were validated by comparison with 4-probe and Hall effect experiments [82].

3.3. Van der Pauw measurements

Hall-effect measurements are performed on rectangular slabs (Hall bars with 4–8 contacts [18]) that are tedious to fabricate on FDSOI wafers. Thanks to Van der Pauw, the Hall-effect theory has been extended to samples of arbitrary shape with 4 peripheral contacts [84]. We use the same square Si islands as for the pseudo-MOS and apply pressure probes in the corners (Fig. 16c). The die is placed on a metal chuck (back-gate) that can be moved into a magnet.

The experimental procedure involves 3 steps:

(a) *Contact verification* – The I–V characteristics of all pairs of contacts are recorded to find the bias range for which their behavior is ohmic.

(b) *Resistivity measurement* – The current I_{12} is injected between two adjacent contacts and the voltage drop V_{34} is detected between the two other terminals. An equivalent resistance $R_{12,34} = V_{34}/I_{12}$ is obtained. Then, the measurement is repeated, by shifting by a quarter turn the contacts, to determine $R_{23,41}$. The film resistivity ρ is given by [9]:

$$\rho = \frac{\pi t_{Si}}{\ln 2} \cdot \frac{R_{12,34} + R_{23,41}}{2} \cdot f \tag{28}$$

where $f = 1$ for symmetrical samples (i.e., $R_{12,34} \approx R_{23,41}$) [9]. For additional accuracy, the measurement is duplicated by injecting the current between probes 3–4 and 4–1. The final resistivity is the average value.

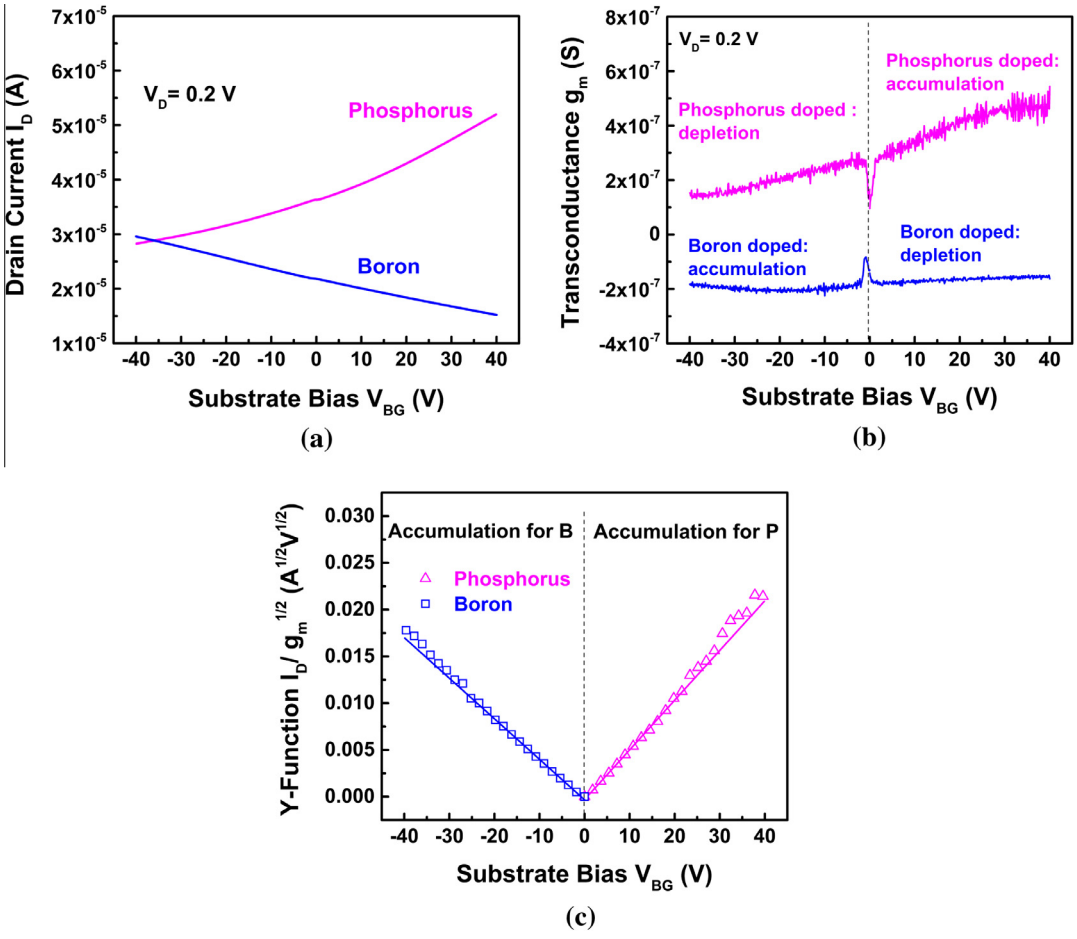

Fig. 22. Drain current (a) and transconductance (b) in 40 nm films doped with boron and phosphorous ($\approx 10^{19}$ cm^{-3}). The non-constant g_m reveals the formation of the accumulation channel which is superposed to the volume contribution. (c) Adapted Y-function for extraction of the flatband voltage and carrier mobility in the accumulation channel (adapted from [82]).

(c) *Carrier mobility and concentration extraction* – A magnetic field B is applied perpendicular to the die. A current I_H is now injected between opposite probes 1–3 and the corresponding voltage V_{24} is recorded. The measurement is repeated by reversing the directions of current *and* magnetic field. The Hall voltage V_H is:

$$V_H = \frac{V_{24}(I_{13}, +B) - V_{24}(I_{31}, +B) + V_{24}(I_{31}, -B) - V_{24}(I_{13}, -B)}{4} \tag{29}$$

The averaging for $\pm B$ eliminates possible magnetoresistance effects and is far more accurate than the comparison to zero field data [9]. A supplementary precaution is to repeat the extraction for a quarter turn shift of the contacts. The average Hall voltage yields the Hall coefficient R_H and Hall mobility μ_H:

$$R_H = -\frac{V_H \cdot t_{Si}}{I_H \cdot B}, \quad \mu_H = \frac{|R_H|}{\rho} \tag{30}$$

The merit of Van der Pauw measurements is to provide independent values of carrier concentration ($n \approx 1/qR_H$) and mobility. The Hall mobility is higher than the drift mobility due to the energy distribution of the relaxation time [9]. In SOI wafers, the resistivity, concentration and mobility are monitored as a function of the back-gate bias. Despite the numerous measurements needed for accurate characterization, the overall step-by-step procedure is relatively fast when computer controlled and automated.

4. Characterization of FDSOI transistors

4.1. Basic parameters and coupling effects

In FDSOI MOSFETs, the depletion charge does not vary with the gate voltage, which enables enhanced control of the inversion charge and current. The front- and back-surface potentials are coupled, meaning that the electrical characteristics of one channel vary with the bias applied to the opposite gate. As a consequence, the front-gate characteristics depend on the back-gate bias and quality of the BOX and interface. This mechanism is called interface coupling. The main electrical parameters of FDSOI MOSFETs (threshold voltage, subthreshold swing and mobility) are affected by inter-gate coupling between front and back channels. The scaling of gate length imposes the thinning of the silicon film and buried oxide, which in turn accentuates the coupling effects.

4.1.1. Threshold voltage

The lateral shift of the transfer $I_D(V_{FG})$ curves with back-gate bias V_{BG} (Fig. 23) is explained by the variation of the front-channel threshold voltage V_{TF} [32]:

$$V_{TF}^{dep} = V_{TF}^{acc} - \frac{C_{Si} \cdot C_{BOX}}{C_{OX} \cdot (C_{BOX} + C_{Si} + C_{it,B})} \cdot (V_{BG} - V_{BG}^{acc}) \tag{31}$$

where C_{Si}, C_{OX}, $C_{it,B}$ are the capacitances of the fully-depleted film, oxide, and interface traps. The subscripts F and B hold for the front or the back channel parameters.

The potential coupling causes the front-threshold voltage to decrease linearly with increasing V_{BG} between two plateaus corresponding respectively to accumulation and inversion at the back interface (Fig. 23). The effect of inter-gate coupling is screened once the back interface is accumulated or inverted. The plateau in region **I** (back-channel inversion) is actually observed only when V_{TF} is measured with the second derivative of drain current (Section 2.1.2) or with the capacitance derivative (Section 2.3.3). Extrapolation of V_{TF} at a given current value would lead to an unphysical sharp decrease (as shown in Fig. 7a). The schematic piecewise V_{TF} (V_{BG}) curve in Fig. 23 corresponds to the pioneering Lim and Fossum model [32]. An updated model [8] and experimental results (see Figs. 7a and 30) show smoother transitions between regions **A**, **D** and **I**.

The actual value of V_{TF} depends on the gate stack and metal work-function. In logic FDSOI CMOS circuits, V_{TF} is set to around 0.3 V at 300 K. Coupling is useful for dynamic tuning of threshold voltage, which is a key advantage of FDSOI. For example, V_{TF} is lowered in ON mode ($V_{BG} > 0$ in n-channel MOSFETs) in order to achieve higher drive current, whereas it is increased in OFF mode ($V_{BG} < 0$) for reducing the leakage current and static power consumption.

The roles of the two gates are reversible: the same generic behavior is observed when the back threshold voltage is plotted as a function of the front-gate bias (Fig. 23).

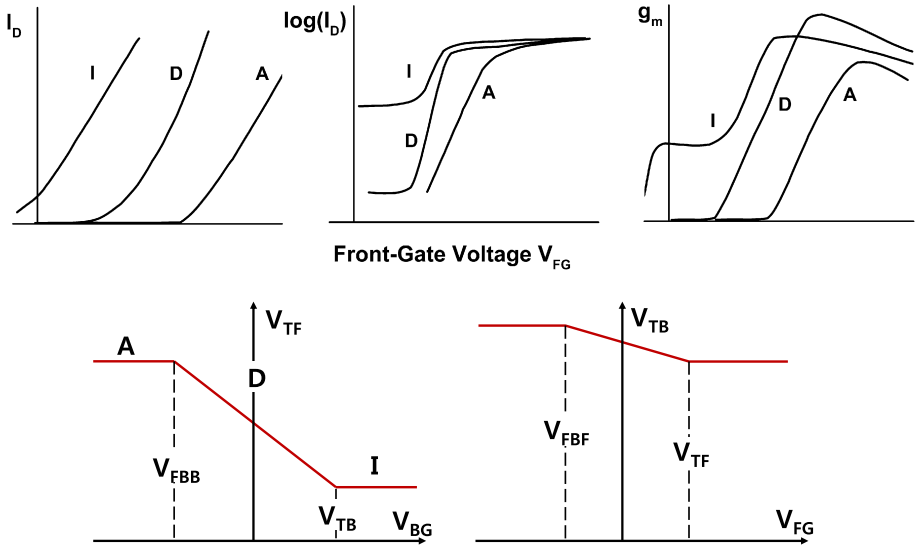

Fig. 23. Generic front-channel characteristics of FDSOI n-channel MOSFET for different conditions at the back interface: accumulation (A), depletion (D), and inversion (I). From left to right, the characteristics are: $I_D(V_{FG})$ in strong inversion, $\log I_D(V_{FG})$ in weak inversion, and the transconductance $g_m(V_{FG})$. The bottom curves depict schematically the variation of the front (back) threshold voltage as a function of the bias applied at the back (front) gate.

4.1.2. Subthreshold swing

The subthreshold slope reflects the MOSFET switching performance. A sharper slope is essential for low-power, low-voltage CMOS: for a given threshold voltage, the OFF current (i.e., static power) is reduced or, reciprocally, at given I_{OFF} the threshold voltage and nominal operating voltage can be lowered. For depletion at the back interface, the subthreshold slope (Fig. 23) is steeper and the subthreshold swing, $SS = dV_G/d(\log I_D)$, is minimum. In FDSOI MOSFETs, the front subthreshold swing (image of the front-channel current in weak inversion) is given by [85]:

$$SS = 2.3 \cdot \frac{kT}{q} \cdot \left(1 + \frac{q \cdot D_{it,F}}{C_{OX}} + \frac{C_{BOX} + q \cdot D_{it,B}}{C_{Si} + C_{BOX} + q \cdot D_{it,B}} \cdot \frac{C_{Si}}{C_{OX}}\right) \quad (32)$$

The impact of front-interface traps $D_{it,F}$ is in principle erased by using ultrathin high-k dielectrics ($C_{OX} \gg qD_{it,F}$). The peculiarity and success of FD devices (SOI, FinFET, nanowires) comes from the last term in Eq. (32), which is intrinsically very small; hence, the swing approaches the thermodynamic limit of 60 mV/decade at room temperature. This term is influenced by the back-interface traps $D_{it,B}$ and BOX thickness. In Smart-Cut SOI, $D_{it,B}$ is typically in the low 10^{11} cm^{-2} eV^{-1} range. Since the BOX is much thicker than both the film and the front-gate oxide, the last term in Eq. (32) can be ignored. For comparison, in bulk or partially depleted MOSFETs, this term is significantly higher being replaced by C_D/C_{OX}. The detrimental effect of the depletion capacitance C_D on the swing is eliminated in FDSOI.

Accumulation at the back channel decouples the front inversion channel from back interface defects but, in turn, this induces a net degradation of the swing (Fig. 23): the reason is that the last term in Eq. (32) becomes C_{Si}/C_{OX}.

4.1.3. Transconductance and mobility

The transconductance curves $g_m(V_{FG})$ in FDSOI MOSFETs have a conventional behavior as long as the back channel does not reach inversion (Fig. 23). The coupling effect shifts the curves laterally (due to V_{TF} change) and modifies the peak value. The transconductance is maximum for depletion at the back interface due to combined effects of reduced vertical field and series resistances [86]. The transconductance curve *I* is distorted, exhibiting a plateau that originates from the premature activation of the back channel: while the front interface is still depleted, increasing V_{FG} reduces the back threshold voltage and opens the back channel before the front channel [86].

The transconductance gives only a rough estimation of the carrier mobility. The field-effect mobility ($\mu_{FE} \sim g_m$) is notoriously affected by coefficients $\theta_{1,2}$ in Eqs. (1)–(5). In particular, large series resistance in θ_1 is responsible for highly underestimated mobility from g_m. Since the transconductance peak does not occur at threshold voltage, the denominator in Eq. (3) cannot be neglected as it is common to assume. In other words, the g_m peak yields intrinsically a pessimistic value of the low-field mobility μ_0. This is why other methods, such as *Y*-function, split-*CV* or magnetoresistance, are recommended for mobility characterization.

In recent FDSOI MOSFETs, the mobility at the front channel is constantly smaller by 30–50% than at the back channel. This result indicates the inferior quality of the Si/high-k interface compared with the Si/SiO_2 BOX interface in Smart-Cut SOI structures. The back-channel mobility is always higher when measured at wafer level with Pseudo-MOSFET than in MOSFETs. This difference is useful on-line to reveal, and possibly solve, the crystal degradation problems induced by the CMOS process.

The coupling effect affects the mobility to such an extent that it can eventually invalidate the use of the popular 'universal mobility' curve (dotted curve in Fig. 24) [87]. The mains reason is that in FDSOI the average vertical electric field can decrease as the inversion charge (i.e., gate bias) increases. A comprehensive situation is illustrated in Fig. 24 where the mobility has been measured by magnetoresistance [51]. The curve is unusual as it features two branches. Can two mobility values correspond to the same effective field? Yes, if the carrier distribution profiles are different, with the charge centroid located near the film–BOX interface for the lower branch and near the front interface for the upper branch. Here the back gate is biased near inversion ($V_{BG} < V_{TB}$), so the increase in V_{FG} reduces the back-threshold voltage V_{TB} by coupling and opens the back channel before the front channel. Point A shows the initial back-channel mobility which increases rapidly with V_{FG} to point B. First, the absolute value of the effective field, initially governed by V_{BG}, is lowered. Second, Coulomb scattering is gradually screened by the forming inversion layer and phonon scattering dominates. After the back-channel mobility has reached a remarkable peak value (550 cm^2/V s at point B, Fig. 24a), the front channel starts conducting as well. The combination of front- and back-channel mobilities results in a mild second peak (point C). In the high field region, definitely governed by the front-gate bias, the mobility decreases (point D) due to prevalent surface-roughness scattering. More or less similar double-branch mobility curves have been produced by split-*CV* measurements [88]. Remark that the notion of 'front-channel mobility' or 'back-channel mobility' becomes obsolete; 'mobility viewed from the front- or back-gate' is preferable as it encompasses both.

We conclude that the action of the back-gate bias on the mobility is two-fold: modification of the vertical electric field and shift of

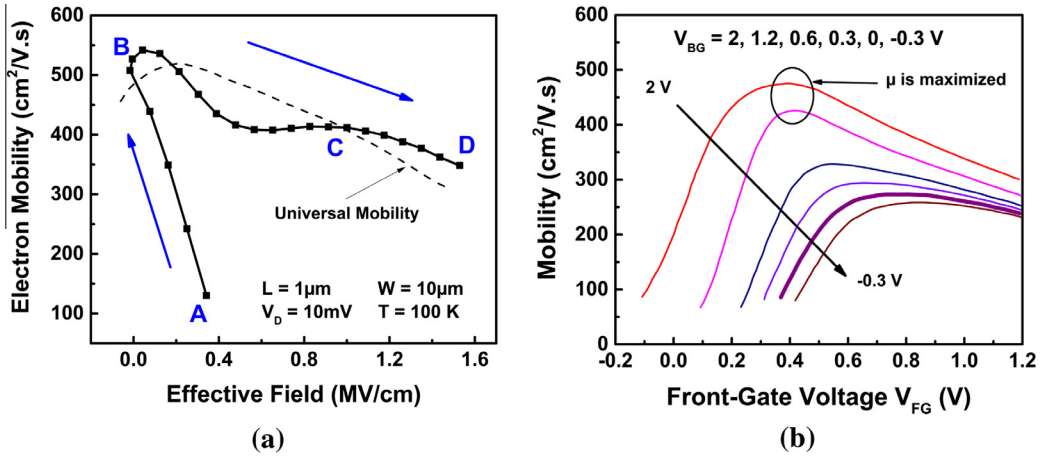

Fig. 24. (a) Magnetoresistance electron mobility versus effective field (at V_{BG} = +20 V) in FDSOI MOSFET with 10 nm film, 145 nm BOX and 1 μm gate length (after Chang et al. [51]). (b) Electron mobility, determined using the split-CV method, versus front-gate bias in FDSOI MOSFET with 8 nm film and 10 nm BOX (after Ohata et al. [89]).

the carrier distribution from the top interface to the less defective Si–BOX interface. An example of practical interest is shown in Fig. 24b. Compared with the case of grounded substrate (bold curve, Fig. 24b), a small positive voltage on the back gate enhances the mobility by a factor of two whereas a negative bias decreases it. Bias engineering of carrier mobility is a simple method that adds to the V_T tuning scheme: positive bias on the ground plane lowers V_T and simultaneously improves the mobility, both effects contributing to a higher current in ON-state [88].

The highest mobility is measured when the carrier centroid is located in the middle of the film, such as surface scattering is minimized. This case, which occurs naturally in double-gate FinFETs, can also be emulated by operating FDSOI MOSFETs in double-gate mode: $\Delta V_{BG} = (t_{BOX}/t_{OX})\ \Delta V_{FG}$, i.e., the inversion charges in the front and back channels are balanced. A gain in low-field mobility above 30% is achieved as compared with the regular single-gate operation [90].

4.1.4. Interface traps

Front- and back-gate measurements (subthreshold swing, charge pumping or noise) can in principle yield the density of traps at each interface. This is no longer the case in FDSOI MOSFETs where the two interfaces are coupled and their discrimination becomes complicated. For example, Eq. (32) indicates that the front-channel swing actually depends on the trap concentrations at both interfaces. In practice, $D_{it,F}$ cannot be determined from the swing because the capacitance of the high-k dielectric is overwhelming. For 1 nm EOT, a change in $D_{it,F}$ of 4×10^{11} cm^{-2} eV^{-1} increases the swing by only 1 mV/decade which is very difficult to detect.

A possible, rather surprising solution is to measure the back-channel subthreshold swing given by the reciprocal of Eq. (32) (with interchanged subscripts). Normally, $D_{it,B}$ is small enough to be offset by the BOX capacitance; hence the back-channel swing reflects to some extent the contribution of $D_{it,F}$ [91]. The coupling curve $V_{TB}(V_{FG})$ also contains $D_{it,F}$ (reciprocal of Eq. (31)), but again the extraction is tedious and unconvincing. Charge pumping and noise measurements, together with appropriate coupling models, stand as more reasonable characterization methods for interface traps.

4.2. Impact of scaling-related mechanisms

4.2.1. Typical short-channel effects

The scaling of FDSOI MOSFETs is based on body thinning. Electrostatic models, experimental results and simulations revealed that Short-Channel Effects (SCE) are kept under reasonable control if the body thickness is 4 times smaller than the gate length [92]. The interplay between short-channel and ultrathin-body effects is a unique feature of FDSOI that requires special attention.

4.2.1.1. Threshold voltage roll-off and subthreshold slope degradation. In short MOSFETs, the body is no longer controlled entirely by the gate. The lateral depletion induced by source and drain terminals weakens the gate control which results in threshold voltage reduction (roll-off) and subthreshold swing degradation. Roll-off can be counteracted by overdoping the channel extremities (halos) or by further film thinning. The latter strategy is very efficient as shown in Fig. 25 [93]. Reducing the temperature of operation makes the subthreshold slope steeper ($SS \sim T$), whereas the threshold voltage is increased quasi-linearly ($\Delta V_{TF}/\Delta T \sim -0.7$ mV/K).

4.2.1.2. Drain-Induced Barrier Lowering (DIBL). DIBL accounts for the decrease in threshold voltage as the drain bias increases, due to the lowering of the source-to-body injection barrier. A more severe

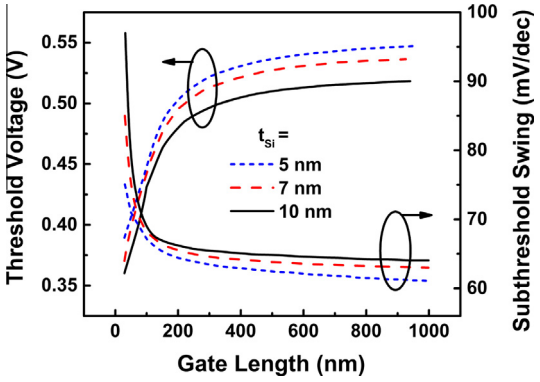

Fig. 25. Effect of Si film thickness on threshold voltage roll-off and subthreshold swing degradation in short FDSOI MOSFETs. V_D = 20 mV, V_{BG} = 0 V (after Chang et al. [93]).

effect in FDSOI MOSFETs is DIVSB (drain-induced virtual substrate biasing). DIVSB reflects the penetration of the electric field from drain through BOX and substrate [94,95]. This fringing field acts as a virtual back-gate with positive bias and raises the potential at the film–BOX interface. The threshold voltage V_{TF} is lowered via coupling effect. DIBL and DIVSB effects combine together and cannot be discriminated by single-device measurements. Benchmarking of transistors with different architectures shows that DIBL is effectively reduced by film thinning, whereas DIVSB decreases in MOSFETs with thinner BOX and ground plane.

Measurements show that the usual DIBL criterion, $\Delta V_{TF}/\Delta V_D \leqslant 100$ mV/V, is easily achieved for 14-nm-node transistors with 20 nm gate length, 6–7 nm film and 20 nm BOX [96]. Further device thinning (t_{Si} = 5 nm and t_{BOX} = 7.5 nm) ensures the scalability of FDSOI MOSFETs down to 10 nm gate length and probably beyond. Reverse back biasing ($V_{BG} < 0$ in n-MOS) is an additional tool to further reduce DIBL [97].

4.2.2. Thickness and channel length effects on mobility

Fig. 26a shows a strong mobility reduction in FDSOI as the channel length shrinks. Such mobility degradation has been extensively reported in other technologies and at least three arguments are under debate.

(i) *Ballistic transport.* In quasi-ballistic operation, the drain current, $I_D \sim v_{th} \cdot Q_{inv}$, would be governed by the thermal velocity ($v_{th} \sim \sqrt{kT/m} \approx 10^7$ cm/s) and independent on channel length. By referring to the standard current equation, $I_D \sim (\mu/L)\ Q_{inv}$, a 'ballistic' mobility, obviously proportional with L, can be defined: $\mu_{bal} = qv_{th}L/2kT$ [98,99]. Nevertheless, μ_{bal} is too large in Si compared to the experimental mobility μ_{exp}. Applying the Matthiessen law

$$\frac{1}{\mu_{exp}} = \frac{1}{\mu_{bal}} + \frac{1}{\mu_{dd}} \tag{33}$$

it is found that the actual drift-diffusion mobility μ_{dd} is slightly higher than the experimental mobility. Unlike for high-mobility semiconductors [98], where μ_{dd} is the value measured in long channels, in FDSOI the correction for ballistic effects is small and cannot explain why both μ_{exp} and μ_{dd} heavily decrease with L [99,100].

(ii) *Localized defects.* It is known that the implantation of source and drain terminals and/or the processing of the gate stack results in defects located near the gate edges. These narrow defective regions are prone to enhanced carrier scattering. In long transistors, the mobility is hardly affected but, as the

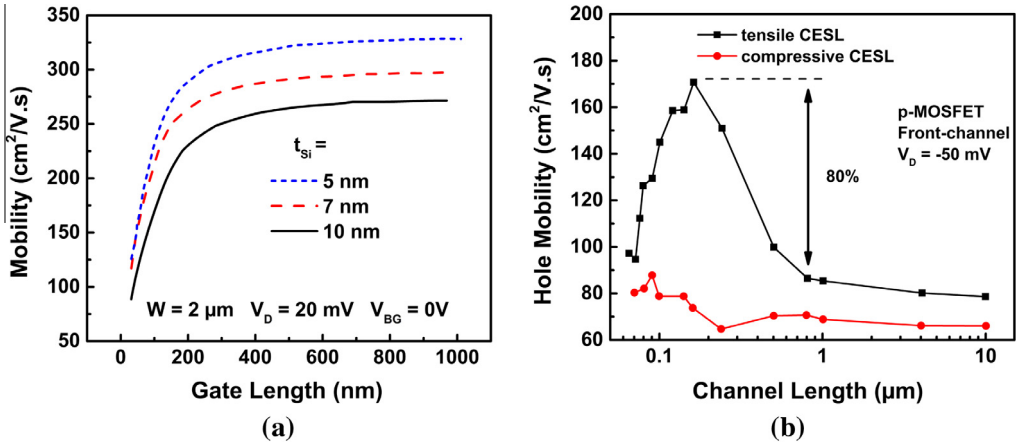

Fig. 26. (a) Effect of gate length and film thickness on electron mobility in FDSOI MOSFETs (after Chang et al. [93]). (b) Hole mobility versus gate length in FDSOI MOSFETs with compressive CESL strain (after Loan et al. [100]).

gate length decreases, the two defective 'edge' regions tend to overlap, leading to an increased effective density of defects that lowers the mobility.

(iii) *Gate-dependent series resistance and effective channel length.* Most FDSOI MOSFETs feature gate-underlapped structure with low doped or undoped source/drain extensions, used to optimize the series resistance vs. SCE tradeoff. As documented by Fossum and Trivedi [8], the gate modulates the potential not only in the channel but also in the extension regions. Hence, the series resistance R_{SD} and the effective channel length are bias dependent ($L_{eff}(V_G) \geqslant L_G$). Accounting for $R_{SD}(V_G) \sim (V_G - V_T)^{-1}$ in the drain current expression (2) results in a mobility formulation similar to Eq. (33), where μ_{bal} is replaced by a term proportional to L_{eff} [101]. This term enables reproducing the experimental mobility collapse $\mu_{exp}(L)$.

Additional information is gained from measurements at low-temperature, where the mobility is higher. Since phonon scattering is attenuated, the other scattering mechanisms (Coulomb, edge defects, surface roughness) are easier to discriminate. The usual mobility-temperature dependence, $\mu \sim T^{-\alpha}$ (with $\alpha \approx 0.7$–1.5 according to the technology), is observed only in long channels. In very short MOSFETs, the mobility can even saturate when scattering on neutral 'edge' defects prevails. Note also that the temperature behavior of front and back mobility can be different since the scattering mechanisms are not necessarily the same.

Strain is an efficient booster of carrier mobility in FDSOI. Bi-directional strain is an option offered in sSOI Smart-Cut wafers. Device fabrication can turn it into unidirectional strain if the transistor is very narrow or very short. Additional strain can be induced during the CMOS process: longitudinal strain by source–drain engineering with SiGe or SiC that have different lattice constants, lateral strain from shallow trench isolation, and vertical strain from either strain memorization techniques or CESL (Contact Etch-Stop Layer). The outstanding benefit of compressive CESL strain in 100 nm long p-channel FDSOI MOSFETs is shown in Fig. 26b: hole mobility is increased by 80% [100].

The mobility variation with channel length indicates the localization of CESL strain at the channel ends, as confirmed by mechanical simulations. This is why in a long MOSFET, where most of the channel remains unstressed, there is no mobility gain. The overlap of the strain regions maximizes the stress and leads to a remarkable mobility peak. However, in transistors shorter than 100 nm the mobility drops as a result of competing effects of strain, neutral defects, and Coulomb scattering in the source/drain depletion regions, which all become very effective. The combination of these scattering mechanisms, non-uniform along the channel, with a Matthiessen rule as in Eq. (33) can match the experimental $\mu(L)$ data [100].

The *thickness* effect is specific to FDSOI and has generated controversial reports. Many results showing a mobility degradation in sub-20 nm thick MOSFETs can be explained by the immaturity of the CMOS process (film thinning by sacrificial oxidation, high-k interface, etc.) and/or the inadequacy of the characterization methods to cope with the highly increased series resistance. Recent measurements in the 4–16 nm range reveal rather constant mobility (Fig. 27a). Theoretical considerations together with Monte Carlo simulations actually predict a mobility peak at ~3 nm thickness, due to the electron redistribution between subbands with different effective mass [102,103]. Measurements at low temperature eliminate phonon scattering and confirm this mobility maximum [104]. Only in films thinner than 2–3 nm does the mobility degrade dramatically ($\mu \sim t_{Si}^6$) as a result of carrier and phonon confinement, thickness fluctuations and surface roughness [105].

There is however an intrinsic mechanism responsible for mobility lowering with thickness. While in bulk MOSFETs the vertical field is entirely governed by the gate, in FDSOI an additional field component ($\sim(\Psi_{sF} - \Psi_{sB})/t_{Si}$) is induced by the difference between front- and back-surface potentials $\Psi_{sF,B}$. The effective mobility in Eq. (5) can be corrected as [106]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 \cdot (V_G - V_T)} \cdot \frac{1}{1 + \alpha \cdot \frac{\Psi_{sF} - \Psi_{sB}}{t_{Si}}} \tag{34}$$

where $\alpha = 7.5 \cdot 10^{-6}$ cm/V.

The *Y*-function accounts for the effect of gate bias exclusively and yields the 'mobility at low gate-induced field', μ_{G0}, which is smaller than the conventional low-field mobility μ_0: $\mu_{G0} = \mu_0/[1 + \alpha(\Psi_{sF} - \Psi_{sB})/t_{Si}]$. The extracted mobility μ_{G0} naturally decreases in thinner films due to the higher intrinsic field. The worst case occurs when the front channel is in strong inversion ($\Psi_{sF} = 2\Phi_F$) and the back channel is driven towards accumulation ($\Psi_{sB} \approx 0$). The intrinsic field is roughly $2\Phi_F/t_{Si}$ and increases by one decade, reaching 0.8 MV/cm, as the film is thinned down from 70 nm to 7 nm. According to the universal mobility curve [87], the effective mobility is severely degraded by ~50%, even if the crystal and interface quality is unchanged. Eq. (34) also explains why the measured mobility is higher when the back channel is driven into inversion ($\Psi_{sF} - \Psi_{sB} \approx 0$). For depletion at the back interface, the mobility varies linearly with V_{BG} mimicking the variation of $\Psi_{sB}(V_{BG})$ [106].

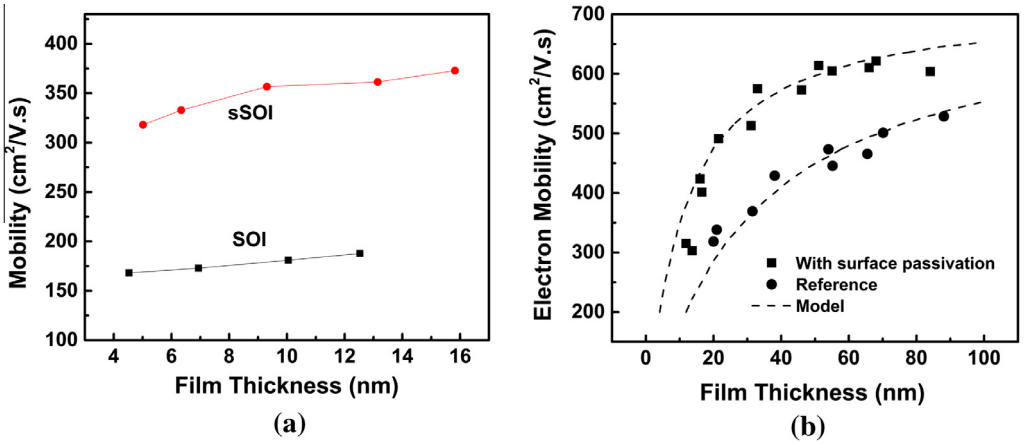

Fig. 27. Electron mobility versus film thickness in (a) FDSOI MOSFETs (after Nguyen [107]) and (b) pseudo-MOSFETs with passivated or unpassivated surface (after Hamaide et al. [106]).

The scaling of the intrinsic field should be considered when examining the mobility-thickness variation in FDSOI. The degradation of the 'low-field mobility' in thinner films is an artefact of the *Y*-function. This function is expected to deliver the low-field mobility but cannot because the field is not 'low' at all in ultrathin films. The mobility is merely shifted along the 'universal mobility' curve due to the intrinsic field. Although the low-field mobility cannot be measured, its actual value μ_0 is derived from Eq. (34), and does not depend on thickness [106].

Pseudo-MOSFET measurements show the same trend of mobility reduction in thinner films (Fig. 27b). In bare SOI wafers, the native oxide and related surface charge induce high vertical field. Wafer surface passivation lowers the density of defects and the intrinsic field, leading to visible improvement in mobility. The dotted lines, calculated with Eq. (34) by simply changing the top surface potential Ψ_{sF}, match convincingly the experimental data [106]. They show no change in μ_0 value with thickness which denies any speculations about film damage during thinning.

4.2.3. Overestimation of short-channel effects in FDSOI

The down-scaling of the body thickness is required to keep/improve the control of the short channel by the gates. State-of-the art devices with buried oxide thinner than 25 nm revealed new interest in back-biasing schemes for tuning the threshold voltage [108,109] and mobility [88,89]. It is less known that inter-gate coupling leads to the overestimation of SCE that are conventionally attributed to the weaker control of shorter channels by the front gate. This view is too simplistic in FDSOI.

The threshold voltage is usually measured as a function of channel length by keeping the back-gate grounded (Fig. 28). However, the threshold voltage roll-off occurs not only at the front channel (ΔV_{TF}) but also at the back channel (ΔV_{TB}).

When the gate length is reduced, the front-surface potential induces a 'primary' front-gate threshold voltage drop ΔV^*_{TF}. In the meantime, the back-surface potential is increased by (ΔV_{TB}). This is equivalent to a positive back bias (albeit $V_{BG} = 0$) which further lowers V_{TF} by the gate coupling 'domino' effect. Therefore, the measured front threshold voltage roll-off (ΔV_{TF}) is a contribution of the genuine roll-off due to the SCE at the front interface (ΔV^*_{TF}) plus the coupling-induced term originated from the back gate ($\alpha_{FG} \cdot \Delta V_{TB}$) [110]:

$$\Delta V_{TF} = \Delta V^*_{TF} + \alpha_{FG} \cdot \Delta V_{TB} \tag{35}$$

where α_{FG} represents the coupling coefficient, calculated from Eq. (31):

$$\alpha_{FG} = \frac{dV_{TF}(V_{BG})}{dV_{BG}} = \frac{C_{Si} \cdot C_{BOX}}{C_{OX} \cdot (C_{BOX} + C_{Si} + C_{it,B})} \approx \frac{t_{OX}}{t_{BOX}} \tag{36}$$

The genuine $\Delta V^*_{TF}(L)$ curve can be evaluated by adjusting the back-gate bias for each length, $V_{BG}(L) = -\Delta V_{TB}(L)$, such as to maintain the back-surface potential nearly constant [110]. The comparison of 'as measured' and corrected curves in Fig. 28a shows that coupling is

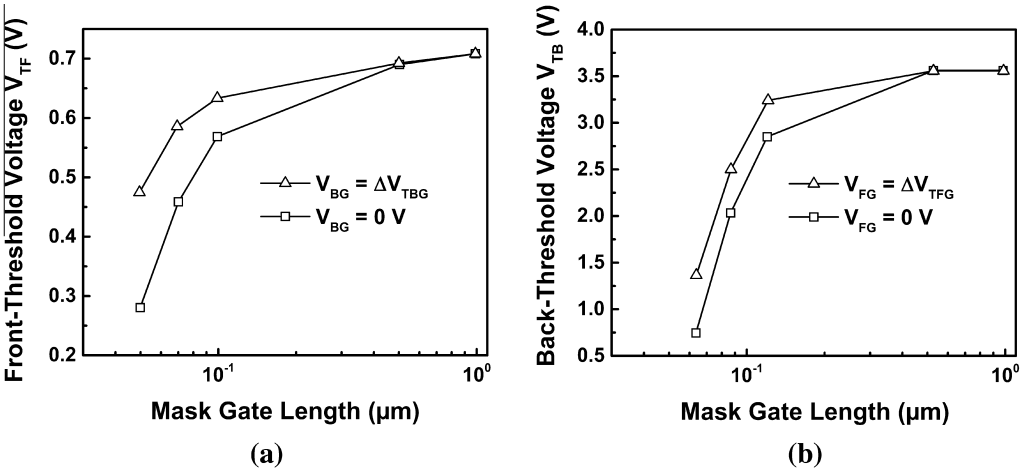

Fig. 28. Experimental (a) front-gate and (b) back-gate threshold voltage roll-off as a function of the gate length for SOI nMOSFETs with $N_A = 2 \times 10^{17}$ cm^{-3}, $t_{OX} = 4$ nm, $t_{Si} = 26$ nm and $t_{BOX} = 25$ nm.

responsible for 50% of the apparent roll-off. A similar mechanism affects the DIBL.

This amplification of SCEs through the inter-gate coupling has escaped attention. We conclude that SCE sensed at one interface are reinforced by the SCE at the other interface: they are overestimated when exclusively attributed to one gate and not to the combination of the SCE that each gate experiences.

This parasitic feedback effect has however interesting applications among which the dynamic tuning of the threshold voltage [108]. A wise back-gate biasing strategy can be used to partially or fully suppress the SCE influence from the opposite gate [110,111]. The adjustment of the threshold voltage is very attractive since the modulation of SCE is implicit when modifying the back-gate bias, further improving the power consumption by the adaptation of the I_{ON}/I_{OFF} current. For negative V_{BG}, SCE are reduced and V_{TF} remains high, keeping I_{OFF} under control. Conversely, a positive V_{BG} increases the SCE and lowers V_{TF} for the benefit of ON current.

4.2.4. Supercoupling

Gate coupling becomes more pronounced as the Si-film is thinned down leading to the extreme case of 'supercoupling' [33]. It occurs when the Si-film is thinner than a critical thickness, $t_{Si} < t^*_{Si}$. Below this critical value, the potential drop across the Si body is not large enough to sustain simultaneously both electron and hole channels. The body then behaves as a quasi-rigid potential well (Fig. 29) where one of the gates prevails. Usually, this implies that the thinnest gate (i.e., the front-gate) drives the entire Si-film. Not only the front-channel but also the back-channel tends to follow the front-gate voltage instead of being independent. For gate voltage V_{FG} close or higher than threshold, electrons will spread in the whole body (volume inversion) even if the back-gate bias V_{BG} is negative. The coexistence of electrons and holes would require voltages beyond the breakdown capability of oxides and film.

Supercoupling is an intrinsic size effect, occurring with body thicknesses in the sub-10 nm range. FDSOI technological parameters (gate stack, BOX thickness) and biases can modify the critical Si-film thickness. The impossibility to accommodate electron channel together with hole channel has several major consequences:

(i) The independent characterization of one interface by accumulating the opposite channel [9] becomes impossible simply because the channels cannot be decoupled.
(ii) The operation of most capacitorless DRAMs is based on the coexistence of electron and hole channels. These memory cells need a body thicker than the critical thickness.
(iii) The dynamic threshold voltage control [112] is achieved by negatively biasing the back gate to increase V_{TF} in off-state. The $\Delta V_{TF}/\Delta V_{BG}$ modulation stops when the accumulation layer is formed and blocks the back-surface potential. In FDSOI MOSFETs with sub-critical thickness, the tuning range is expanded, being no longer limited by the formation of the back accumulation layer (Fig. 30a).

The supercoupling as a 2D effect is evidenced experimentally by extracting the threshold voltage in SOI devices with different Si-film thicknesses and channel lengths [113]. Accumulation at the back interface is detected when $V_{TF}(V_{BG})$ curve exhibits a flat region. This plateau is associated with the accumulation of holes that blocks the impact of the back-gate bias on the front-channel. The absence of the plateau indicates that supercoupling is taking place (see curve for t_{Si} = 7.8 nm in Fig. 30a).

Even if very thin silicon film devices are more resilient against SCE, supercoupling remains actually a 2D effect amplified in short-channel SOI MOSFETs (Fig. 30b). Indeed, when the channel length is reduced, the body potential is slightly increased due to the proximity of source/drain junctions. As a consequence, the back bias required to reach accumulation becomes more negative i.e., the critical film thickness is virtually increased.

4.2.5. Floating-body effects in FDSOI

In SOI MOSFETs, the gates, the source- and drain-body junctions isolate electrically the body. Depending on the bias applied, the lack or excess of majority carriers generated within the body leads to out-of-equilibrium body potential variations. This transient behavior specific to SOI technology may induce parasitic effects deteriorating the output electrical characteristics. This problem does not exist in bulk or body-contacted devices, where the majority carrier concentration is maintained at equilibrium by the body contact. The resulting substrate current is typically used to determine the origin of the majority carrier generation (SRH, impact ionization, BTBT) and to extract related parameters (carrier lifetime, trap density, etc.). In FDSOI, the majority carrier current cannot be probed directly and specific transient-current techniques are required (see Section 2.4.3).

4.2.5.1. Kink effect. The classical floating-body mechanisms are triggered by the charging of the body with majority carriers generated by impact ionization [114,115]. This leads to an increase in body potential and a reduction in the threshold voltage. The kink effect denotes a sudden jump in drain current output $I_D(V_D)$

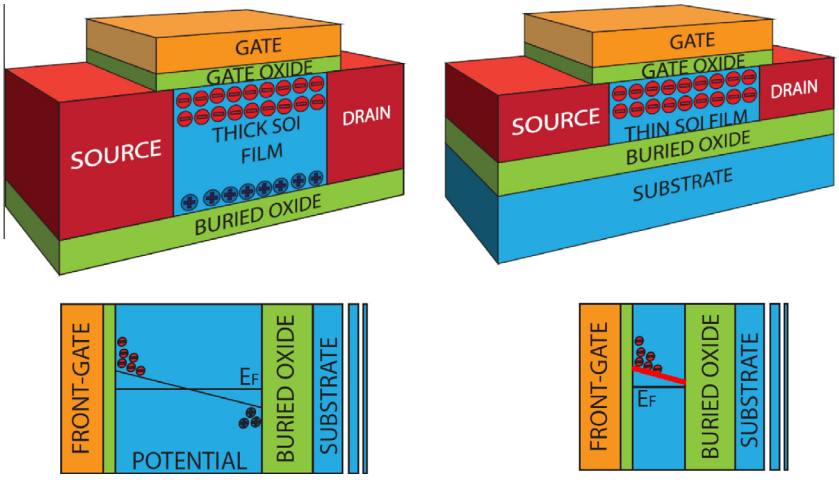

Fig. 29. 2D carrier distribution within the body. Electrons and holes co-exist in thick-body SOI transistors (left). In ultra-thin FDSOI, supercoupling effect inhibits the simultaneous presence of electron and hole layers.

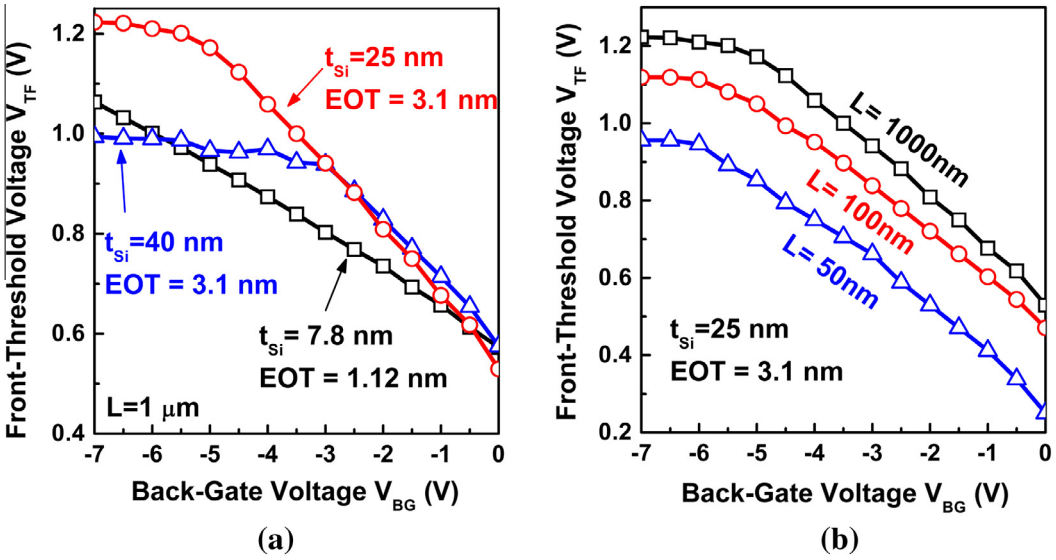

Fig. 30. Experimental evidence of 2D super-coupling effect in n-channel FDSOI MOSFETs. The threshold voltage V_{TF} is plotted as a function of the back-gate voltage to highlight (a) the influence of silicon thickness and (b) channel length (adapted from [113]).

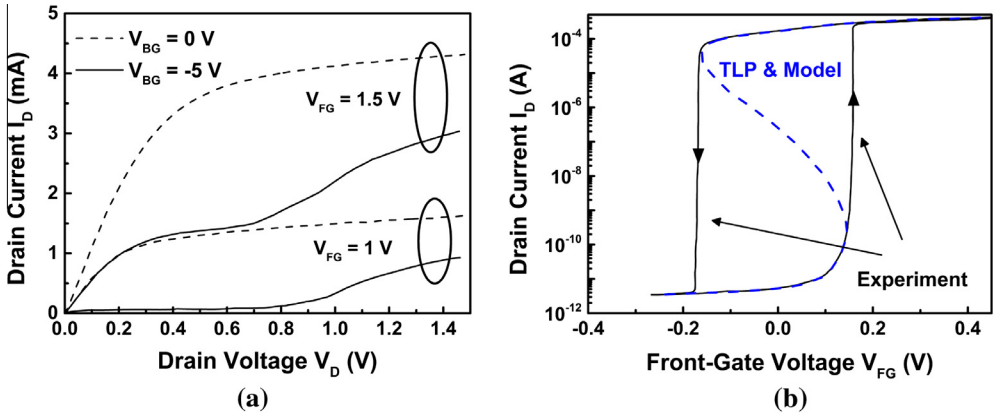

Fig. 31. (a) Output characteristics of long (150 nm) and moderately thin (t_{Si} = 25 nm, t_{BOX} = 25 nm) n-MOSFET showing the activation of the kink effect by back-gate biasing. (b) Hysteresis in transfer characteristics due to body charging [119,120]. The dotted line is recorded with Transmission Line Pulse (TLP) measurements and modeled by the negative transconductance theory [119]. A higher drain bias enlarges the hysteresis window until the device is totally locked in ON mode (latch).

characteristic (Fig. 31a) and in low-frequency noise [116,117]. Even if this effect is considered as marginal in FDSOI MOSFETs [118], it cannot be neglected.

Fig. 31a shows the characteristics of a relatively long MOSFET (150 nm) with 25 nm thick body: the kink effect is absent for V_{BG} = 0 but can be easily turned on with a negative back-gate bias that facilitates the accumulation of holes. In 7 nm thick FDSOI MOSFET, the output characteristics remain kink-free even for negative gate bias (not shown). The difference is explained by the supercoupling effect which inhibits the accumulation of majority carriers in the body.

4.2.5.2. Hysteresis and Latch. The body charging is particularly effective in weak inversion where the current depends exponentially on potential. As the current increases, more electrons contribute to impact ionization and more majority carriers are stored in the body, further increasing the potential. This positive feedback mechanism leads to abnormally low values of the swing (below 60 mV/decade at 300 K, Fig. 31b). For very high drain bias, the body charge is considerable and sustains the inversion channel even when the gate is turned off. This extreme effect, named

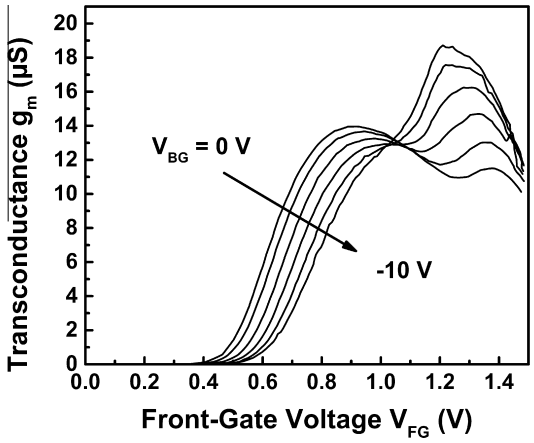

Fig. 32. Transconductance versus gate voltage in FDSOI n-channel MOSFET showing the impact of GIFBE, namely the transconductance increase and the metamorphosis of the double-peak curve into a single-peak curve. This peak defines the body potential increase instead of the low-field mobility. 1.6 nm gate oxide, 17 nm film, and 145 nm BOX, V_D = 0.1 V (adapted from Cassé et al. [123]).

transistor latch [119–121], is responsible for hysteresis in $I_D(V_G)$ and $I_D(V_D)$ characteristics (Fig. 31b) that may be useful for conceiving memory [122] and ESD-protection devices.

4.2.5.3. Gate-induced floating-body effect. In MOSFETs with ultrathin (<2 nm) oxide, the gate tunneling current becomes relevant and can charge the body with majority carriers. The body potential, defined by the balance between the incoming gate tunneling current and the outgoing current (body discharging via junction leakage and carrier recombination), increases with gate voltage. In FDSOI MOSFETs (Fig. 32), the raise of the potential at the film–BOX interface lowers, by coupling effect, the front-channel threshold voltage [123]. Thanks to this gate-induced floating-body effect (GIFBE), the drain current benefits from a double action of the gate: regular increase of the inversion charge and simultaneous decrease of threshold voltage. This mechanism reminds the 'dynamic threshold voltage' operation of transistors with body and gate interconnected.

In practice, GIFBE is detected through the onset of a second peak in transconductance (for $V_{GF} \approx 1.2$ V in Fig. 32). A more negative substrate bias drives the back interface towards accumulation, where the floating-body effects are reinforced. The GIFBE peak gradually increases and offsets the mobility-related initial peak until the double-peak curve transforms into a single-peak curve [123]. In this case, the transconductance maximum is no longer governed by the carrier mobility, but by the body potential; it is clear that the mobility extracted from the transconductance peak is meaningless. In case where the transconductance peak suggests enthusiastic values of mobility, it is highly recommended to verify the results by checking the gate current.

4.2.5.4. Self-heating. The BOX thermal conductivity is two orders of magnitude poorer than in silicon, which inhibits heat dissipation and results in the body temperature rise. The amount of self-heating is evaluated by comparing *dc* and *ac* $I_D(V_D)$ curves. In *dc* mode, the current is smaller (due to the mobility drop at high temperature) and can even exhibit a negative output conductance. But if the V_D pulse is shorter than the time constant of self-heating, the $I_D(V_D)$ characteristics remain unaffected.

In situ temperature measurements require especially patterned MOSFETs where the gate, used as a temperature sensor, has two (or four) independent contacts. The gate resistance is calibrated as a function of temperature using a hot chuck. During transistor operation, the gate resistance is monitored which indicates the gate temperature variation with bias [124]. Temperatures in excess of 100 °C have been reported according to the dissipated power. The *body* temperature can be measured by applying the same principles to transistors featuring two independent body contacts.

4.2.5.5. Parasitic bipolar transistor. The lateral bipolar $N^+P^-N^+$ transistor is intrinsic in n-MOSFETs and becomes effective in short-channels (i.e., narrow base), either partially or fully depleted. It is triggered by impact ionization or band-to-band tunneling currents which lead to the forward biasing of the base/emitter (body/-source) junction. A large collector (drain) current is generated, enhancing the original contribution of the MOS channel. The parasitic bipolar is effective in OFF state and may induce a premature breakdown, in both partially- and fully-depleted transistors [125]. The solutions for attenuating the parasitic bipolar action are based on lifetime killing and source engineering: lightly doped drain to reduce the impact ionization and bipolar gain, source silicidation, etc. [126].

Different methods for the extraction of the bipolar gain β have been proposed. In FDSOI devices with sub-10 nm thickness, the comparison of drain leakage (measured at $V_{FG} < 0$) between short- and long-channels yields $\beta(L)$ [127,128]. A more convenient method, using a single device, is based on back-gate biasing. For relatively high negative V_{BG}, the energy barrier at emitter-base junction is enhanced and the bipolar effect is fully suppressed. The bipolar gain is measured by comparing the leakage currents at $V_{BG} = 0$ and $V_{BG} \ll 0$. Recent results in 30 nm long, 10 nm thick FDSOI MOSFETs showed that the bipolar effect is triggered by band-to-band tunneling (base current) and the gain can exceed 100 [128]. The bipolar mechanism tends to vanish in 5 nm thick transistors where the carrier recombination rate, dominated by interfaces, is highly increased.

5. Conclusions

The characterization of ultrathin FDSOI materials and devices is challenging as it implies the adaptation of experimental setup and interpretation. This paper compiles most effective techniques, from elementary to sophisticate. While the pseudo-MOSFET method is unchallenged for material evaluation, MOS transistors and diodes are invaluable inspection tools for assessing and optimizing the CMOS process. Most of the above techniques can be tuned for implementation in multi-gate nanowires and FinFETs.

Instead of limiting to 'blind' characterization, we opted to show the link between the various methods and the background physics mechanisms. Short-channel, thin-body, strain, coupling and floating-body effects often lead to properties unheard of in bulk silicon. Typical parameters extracted from recent experimental data were discussed with the aim of revealing the main features of state-of-the-art FDSOI structures and their impact on the performance of CMOS devices.

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